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82-1484

No. -

In the Supreme Court of the United States

OCTOBER TERM, 1982

CORDIS CORPORATION,
PETITIONER,

v.

CARDIAC PACEMAKERS, INC.,
RESPONDENT.

APPENDIX TO PETITION FOR WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE EIGHTH CIRCUIT

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United States Court of Appeals
For the Eighth Circuit

No. 81-2048

CARDIAC PACEMAKERS, INC.,
APPELLEE,

v.

CORDIS CORPORATION,
APPELLANT.

ON APPEAL FROM THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF MINNESOTA

Before Ross, *Circuit Judge*,
STEPHENSON, *Senior Circuit Judge*,
and VAN PELT,* *Senior District Judge*.

Submitted: March 25, 1982
Filed: October 12, 1982

PER CURIAM.

This is a patent case brought by Cardiac Pacemakers, Inc. (C.P.I.) against Cordis Corporation (Cordis) in the United States District Court for the District of Minnesota, Fourth Division. After a trial, the Honorable Edward J. Devitt entered what is termed a memo opinion and judgment finding in favor of C.P.I. and against Cordis. Cordis has appealed to this court. We affirm the trial court.

*Robert Van Pelt, Senior District Judge, District of Nebraska, sitting by designation.

Involved is the patentability of devices known as cardiac pacemakers, and particularly of implantable cardiac pacemakers. Originally involved were patents known as the Keller patent, U.S. Patent No. 3,557,796; the Terry patent, U.S. Patent No. 3,805,769; and the Davies patent, U.S. Patent No. 4,095,603.

The preliminary proceedings are described in Judge Devitt's memorandum and nothing is gained by repeating here the history of the parties' prior litigation. While this case was pending, the Keller and Davies patents were withdrawn. The litigation proceeded only as to the Terry patent granted April 23, 1974. The date of the granted invention as determined by the trial court was July 1, 1970.

Users and others reading the record would recognize this case as involving in part a pacemaker made by C.P.I. known as Medtronic and a pacemaker made by Cordis known as Omnicor. Another major producer of pacemakers, Telectronics, accepted a license from Cordis. This litigation ensued when C.P.I. introduced its product to the public market without obtaining such a license.

The issues on appeal are: (1) whether the district court erred in holding that Herbert Lenzkes was a "prior inventor" of the invention granted in the Terry patent, whereby his work anticipated that invention; (2) whether the district court erred in holding that Robert Wingrove, holder of Patent No. 3,833,005 was also a prior inventor of the invention patented by Terry, whereby his work anticipated Terry's invention. The claim is also made that Wingrove never reduced his device to practice as held by trial court; (3) whether the district court erred in holding that the invention claimed in Terry was obvious to one of ordinary skill in the art.

We have considered these assigned errors. We conclude that little is to be gained from our discussing the details of the Terry patent or the other patents cited by Judge Devitt in his opinion.

The facts are largely undisputed. We find Judge Devitt's conclusions from the facts are reasonable.

The applicable law is really not in dispute. We are satisfied with Judge Devitt's reading and application of what constitutes obviousness. We feel he correctly read and applied the cases relating to prior art.

It is sufficient to say that we have read the entire record and believe that Judge Devitt has well analyzed the pacemakers before him and the patents on which they were based, together with the issues raised herein. If we started in to detail the content of each patent, we would, to a great extent, merely repeat his explanations and findings.

We conclude that his opinion is accurate, scholarly, and does justice between the litigants. Such a result is the goal of all litigation.

Upon the basis of the opinion of Judge Edward J. Devitt filed in this case on September 1, 1981, we affirm.

A true copy.

Attest:

CLERK, U.S. COURT OF APPEALS, EIGHTH CIRCUIT.

UNITED STATES DISTRICT COURT
DISTRICT OF MINNESOTA
FOURTH DIVISION

CIV. No. 4-77-427

CARDIAC PACEMAKERS, INC.
PLAINTIFF,

v.

CORDIS CORPORATION,
DEFENDANT.

Haugen & Nikolai, *Orrin Haugen*, Minneapolis, Minnesota; *Allegretti, Newitt, Witcoff & McAndrews, Ltd.*, *Charles G. Call* and *Brad Hulbert*, Chicago, Illinois; and *Kevin T. O'Malley*, St. Paul, Minnesota, attorneys for plaintiff.

Kenway & Jenney, *Henry D. Pahl* and *Gilbert H. Hennessey*, Boston, Massachusetts; and *Williamson, Bains, Moore & Hansen*, *Malcolm L. Moore*, Minneapolis, Minnesota, attorneys for defendant.

MEMORANDUM & ORDER

This is a patent case involving the patentability of an implantable electronic pacer to control irregular human heart beats. Three hundred thousand such devices manufactured by 27 different companies are sold world-wide each year. Two of the principal producers are arraigned in adversary positions here.

The litigation between these parties commenced when Cordis Corporation (Cordis), a Florida corporation, brought a claim for patent infringement against Cardiac Pacemakers, Inc. (CPI), a Minnesota corporation, in the District of Massachusetts. CPI then commenced this declaratory judgment action against Cordis, and the Massachusetts action was dismissed for lack of venue.

In the first suit brought by Cordis, CPI was charged with willfully infringing United States Patents Nos. 3,557,796 to Keller, et al., and 3,805,769 to Terry et al.

CPI filed this action, seeking a declaration that the Terry and Keller Patents are invalid, unenforceable, and not infringed, by reason of prior invention and obviousness under 35 U.S.C. §§ 102 and 103. Cordis counterclaimed, seeking damages for an injunctive relief against infringement of these two patents, and United States Patent No. 4,095,603, which in the interim, had been issued to Davies. CPI replied, asserting the Davies Patent was invalid, unenforceable, and not infringed.

Upon reissue proceedings instituted by Cordis in the U.S. Patent and Trademark Office on the Keller Patent, the Patent Examiner found that the invention defined by claims 1, 2, 6, 7, 9-11, 13 and 14 of the Keller Patent would have been obvious to a person of ordinary skill at the time the Keller invention was made. This decision was upheld by the Patent Office Board of Appeals and the Court of Customs and Patent Appeals. *In re Keller, et al.*, 642 F.2d 413 (C.C.P.A. 1981). Cordis then amended its counterclaim by withdrawing the Keller and Davies Patents. On the Terry Patent remains in this suit.

The issues were tried to the court April 7, 1981 through April 15, 1981. Briefs have been filed.

The basic issue to be decided is the patentability of the Cordis device. It is the position of CPI that the invention claimed by the Terry Patent was previously made by others and that any difference between it and the prior art was obvious to those having ordinary skill in the art. Because of our disposition of this issue, there is no need to reach the infringement issue.

We deal here with a small electronic battery powered device which is implanted under the skin near and connected to the heart. Its operation is directed by pulse signals from without the body by a second device called a "programmer" through which pulse rate and other changes in implanted pacemaker may be effected.

The claims of the patent in suit are capsulized in the abstract on the face sheet of the January 22, 1973 amended application.

> In the implantable cardiac pacer disclosed herein, various operating parameters are determined or controlled by the information held in a digital storage reister such as a binary counter. The information so held may be varied by means of pulse signals transmitted through the body of a patient within whom the pacer is implanted. Rate-sensing and count threshold control circuits are provided to prevent unintended changes in operating parameters.

A summary and description of the invention is followed by the listing of nine detailed claims.[1]

A more simplified statement of the inventions claimed by Terry is that it is an implantable device with a counter which can be changed a step at a time by magnetic impulses from outside the body to adjust the operation of the implanted device, and also containing a "safety" counter to prevent unwanted changes taking place from spurious signals.

A patent is presumed to be valid, and the burden of proving invalidity rests on the person asserting it. 35 U.S.C. § 282. CPI has carried this heavy burden, *see E.I. DuPont de Nemours* v. *Berkley & Co., Inc.*, 620 F.2d 1247 (8th Cir. 1980), and we are convinced that the invention claimed by the Terry Patent is invalid under 35 U.S.C. §§ 102(g) and 103.

---

[1] Claim 1, representative of the claims following it, provides:

An implantable cardiac pacer comprising: means for detecting pulse signals having predetermined characteristics, which pulse signals can be applied externally of a patient within whom said pacer is adapted to be implanted; a first counter interconnected with said detecting means for selectively counting detected pulse signals; a second counter, controlled by said first counter and also responsive to said pulse signal detecting means for counting detected pulse signals occurring after the count held by said first counter reaches a preselected threshold value; a cardiac stimulation pulse generator having at least one changeable output parameter; and decoding means interconnected with said counter for controlling said output parameter in predetermined correspondence with the value of the count held by said second counter.

The Terry Patent

As originally filed on May 10, 1971, the application for the Terry Patent contained seventeen claims reflecting an implantable cardiac pacer which included a counter for counting externally applied pulses, and means for controlling the operating parameters of the pacer in response to the count held in the counter. The application named Cordis employees Reese S. Terry, Jr. and Gomer L. Davies as co-inventors of the patented subject matter.

The genesis of the claims contained in the original application was a memorandum authored by Gomer Davies on September 21, 1969 and sent to other Cordis personnel. The memorandum begins, "For various reasons (meeting competition, providing a more useful device for the patient, etc.) it is desirable to provide an implantable pacer system (of the standby type) in which the rate can be altered under external control." Plaintiff's Exhibit 49 at 701. In discussing approaches to a method for effecting pacer adjustments, Davies alluded to the basic programming technique ultimately claimed in the Terry patent application and incorporated in the Omnicor pacer marketed by Cordis: "One system. . .comprises a reed switch in the pacer that is repetitively actuated by an external magnet to step an internal circuit electrically through a series of states." Plaintiff's Exhibit 49 at 703.

This basic programming technique is described in the Lopin Patent 3,631,860, issued on an application filed October 27, 1969. That patent describes a programmable pacer that can be externally adjusted through the operation of a monostable magnetic reed switch as the pulsing element for changing the state of a counter comprised of electronic circuits which control the rate of the pacer.

Cordis cited the Lopin Patent to the Patent Office and obtained more narrow claims. The Terry patent application was amended by cancelling nine of the seventeen claims. Cordis stated in its amended application that the remaining claims

defined an invention over Lopin. The remaining claims were directed to a protection circuit in the pacer designed to prevent alteration of the set operating parameters of the pacer by spurious magnetic signals.

Timing of the Terry Invention

Cordis argues that the date of conception for the invention claimed in the Terry Patent is September 20, 1969, the date of the Davies memorandum and that the Lopin Patent is thus unavailable as a prior art reference. We disagree.

The Davies memorandum did not describe or discuss means for preventing inadvertent programming of interference. It merely acknowledges "the rather sticky problem of external excitation of such circuits." Plaintiff's Exhibit 49 at 704. It goes on to state "Pulsed RF signals come naturally to mind, but the circuitry that could receive such signals could also respond to high-level interference." *Id.*

Cordis concedes that the claimed invention as a whole was not conceived until July 1, 1970, the date of a drawing by Reese Terry of the device which included the safety counter. The July 1, 1970 drawing was made in response to a request by Cordis President Dr. Murphy to develop an externally programmable pacer. Within several weeks of that request, Reese Terry made the July 1, 1970 drawing relating to external non-invasive programming.

The concept of using an address code to prevent an accidental reed switch closure from affecting the program circuit was originated by Terry. This code was designed to prevent reprogramming unless a grouping of eight magnetic pulses were received by the pacer. The concept of the address code is claimed in the Terry Patent.

We hold that the earliest date of conception of invention claimed in the Terry Patent is July 1, 1970. It was not until that date that the entire conception was complete:

> The conception of an invention consists in the complete performance of the mental part of the inventive act. All

> that remains to be accomplished in order to perfect the act or instrument belongs to the department of construction, not invention. It is, therefore, the formation in the mind of the inventor of a definite and permanent idea of the complete and operative invention as it is thereafter to be applied in practice that constitutes an available conception within the meaning of the patent law.

Rex Chainbelt Inc. v. *Borg-Warner Corporation*, 477 F.2d 481, 491 (7th Cir. 1973) *quoting*, *Mergenthaler* v. *Scudder*, D.C. Cir., 11 App. D.C. 264 (1897). Davies' mere identification of the problem presented by outside interference with programming of the pacer, particularly in light of the fact that the prevention of accidental reprogramming constitutes an essential part of the invention, is fatal to Cordis' position that the Davies memorandum is the conception of the claimed invention described in the Terry Patent. *See id.* at 491-92. Accordingly, the Lopin Patent is available as a prior art reference.

Validity of the Terry Patent

CPI presented extensive expert testimony concerning the scope and content of the prior art, the level of ordinary skill in the art as of July 1, 1970, and the differences between the prior art and the Terry Patent claims. CPI's expert, Leroy Prohovsky, is an electrical engineer with extensive experience in microelectronics and circuit design techniques. We find that Prohovsky, by virtue of his skill, training, and experience was well qualified to testify on this subject. Cordis declined to call an expert witness to rebut Prohovsky's testimony (Trial Transcript, 711-12). In so doing, we reject Cordis' contention that the scope of the prior art be limited to biomedical implantable stimulators. The scope of the pertinent art in this instance includes the field of electrical engineering in general, and more specifically, the use of both digital and analog circuitry. This finding is consistent with the principle that the concept of the scope of the art must be afforded a wide

latitude. *See, e.g., Cathodic Protection Service* v. *American Smelting and Refining Company*, 594 F.2d 499 (5th Cir. 1979), *see also, Skee-Trainer Inc.* v. *Garelick Mfg. Co.*, 361 F.2d 895 (8th Cir. 1966).

Lenzkes Patent

Prior to July 1, 1970, the Huntington Institute of Applied Medical Research ("HIAMR") of Pasadena, California, and General Dynamics Corporation of Pomona, California, collaborated in the development of an implantable, digital, programmable biostimulator later called the "Telestimulator." HIAMR was founded by Drs. Robert Pudenz and C. Hunter Sheldon for the purpose of engaging in neurologial research. HIAMR pioneered the implantation of electronic devices for nerve stimulation in the treatment of neurological disorders.

The inventor of the Telestimulator, H. H. Lenzkes of General Dynamics Corporation, prepared a report dated February 4, 1970, entitled "A Preliminary Concept for a Versatile Implantable Bi-Directional Nerve Stimulator." At that point, the Telestimulator had been "breadboarded", and the feasibility of the system confirmed. On May 13, 1970 Lenzkes reported in writing that the Telestimulator had been constructed by personnel of General Dynamics. That report contained a detailed description of the design organization of the Telestimulator. With the exception of some differences not relevant here, the report of May 13, 1970 parallels the description of the Telestimulator found in the United States Patent No. 3,727,616, issued to Lenzkes. This report also indicated that the device had been breadboarded using COS/MOS devices manufactured by RCA Company. According to Lenzkes' testimony, the breadboarded design functioned satisfactorily. In a Progress Report dated June 23, 1970, Lenzkes indicated that the device had been built in the laboratory and proof of the concept had been verified.

In October 1970 the first prototype of the Telestimulator was delivered to HIAMR. HIAMR personnel implanted it in a cat for testing purposes on or about November 23, 1970.

The Lenzkes Patent was filed subsequent to the Terry application. The evidence shows, however, that the Telestimulator was fully built and successfully tested prior to July 1, 1970. We find that these facts establish that the Telestimulator was actually reduced to practice prior to July 1, 1970, thus entitling it to priority under 35 U.S.C. § 102(g).

While the Telestimulator was being developed HIAMR and General Dynamics disclosed details of the project to outside persons. On August 6, 1970, personnel from Medtronic, Inc. visited General Dynamics and discussed the Telestimulator with Dr. Pudenz and General Dynamics personnel.

At the Neurological Society Conference held March 5, 1971 in San Antonio, Texas. Dr. Pudenz and E. L. Watkins delivered a detailed presentation regarding the Telestimulator. This conference was attended by Dr. Tarjan, a Cordis Vice President, who later informed Reese Terry, Gomer Davies, Cordis President Dr. Murphy about the Telestimulator work.

In September 1971 Dr. Murphy visited HIAMR and observed an experiment utilizing a cat to demonstrate nerve stimulation. He was also furnished with a detailed technical report entitled "Continued Development of the Sheldon/-Pudenz Biostimulator," which explained the operation of the telestimulator.

Based on the foregoing facts, we hold that the Telestimulator work later described in the Lenzkes Patent was not "abandoned, suppressed or concealed" within the meaning of 35 U.S.C. § 102(g).

Plaintiff's expert Mr. Prohovsky testifed at length in presenting a comparison of the Telestimulator work and the claims set forth in the Terry Patent. The Telestimulator system described in the Lenzkes Patent, and in particular Figure 6 of that

patent, incorporated an implantable stimulator including circuits 48 and 130 for receiving pulses of radio frequency (RF) energy transmitted through the skin from an external transmitter. The Lenzkes design utilizes a 21 bit shift register (132) which corresponds to the Terry counter 31.

Data is entered into the shift register-type counter 132 which ultimately functions as a memory for storing the received pulses. The Lenzkes design further includes a stimulation decoder 136 which comprises a second counter having three separate states. Decoder 136 corresponds to the Terry Counter 43. Controlling the entry of data into the first counter 132 and the second counter 136 is a Mode Logic Circuit 134. When power to the transmitter is turned on, a memory preset signal is applied to the first counter 132 to set all of its stages to a zero state. As the external transmitter feeds RF impulses into the receiver circuits 48 and 130, the Mode Logic Circuit 134 initially causes the pulses to be fed into the 21-bit shift register 132. The leading bit in the string of serial data entering the 21-bit counter following "power-up" is forced to be a binary "1" signal and this signal is called the "data completion pulse." Following the application of 21 clock signals which are counted by the counter (shift register) 132, the "data completion pulse" exits from the shift register 132 and is applied to the Mode Logic Circuit 134. This causes the Mode Logic Circuit to block further data entries into the counter 132 and the subsequently received pulses are instead routed to the 3-state counter 136. The contents of the counter 136, in turn, determine the pulse width and the polarity of the stimulating pulse to be applied to the electrodes 52 and 54.

Prohovsky provided the court with comprehensive and credible testimony comparing the Terry claims with the Lenzkes design. His testimony fully supports the claim comparison chart, plaintiff's exhibit 60, which compels the conclusion that the Telestimulator fully anticipated claims 2, 7 and 8 of the Terry Patent under 35 U.S.C. § 102(g).

Prohovsky also explained the differences between the Terry claims and the Telestimulator. These differences include the use of a RF transmission signal to convey pulse information from the external transmitter in the Telestimulator, as opposed to the use of magnetic field to activate a magnetic reed switch in the Terry Patent. There is no switch debounce circuit in the Telestimulator because, with the use of the RF transmission system, it does not include any switch that requires "debouncing." The debounce circuit would have been necessary in the Telestimulator only if it had employed a magnetic reed switch. Another difference cited is that Counter 31 of the Terry Patent is reset when the reed switch is not receiving pulses at a sufficiently high rate. Shift register 132 is reset upon the application of power to the Telestimulator. Prohovsky credibly and fully identified all differences between the Telestimulator and the Terry Patent in compiling the claim comparison chart. His testimony in this regard is relevant to the consideration of the issue of obviousness under 35 U.S.C. § 103. That matter will be considered more fully below.

The Wingrove Work

Robert Wingrove, an employee of Medtronic, Inc. from 1958 through 1972, testified regarding his development of a digital, programmable implantable cardiac pacer during 1970. This pacer included a protection circuit for preventing accidental reprogramming of the pacer by spurious noises in the external environment.

Wingrove began development of the pacer in 1970, working with new integrated circuit devices called complementary metal oxide semi-conductor ("CMOS") circuits. These circuits were well suited to use in implantable pacers because of their switching characteristics and low power consumption.

Wingrove testified that the devce he developed, as reflected in certain documents dated March 2, 1970 and March 13, 1970 was actually built and sent to a Dr. Chardack for implementation in a dog.

The first prototype of the Wingrove pacer is dated March 25, 1970. This device was actually built and tested. Another prototype was built and tested on or about May 27, 1970.

Wingrove, like others, recognized the need for a safety circuit to prevent accidental reprogramming of the pacer. To this end he developed a technique that utilized an ID pulse of a certain width which had to be presented to the implanted unit in order to open a gate to allow reprogramming.

A patent application for the Wingrove device was filed on July 26, 1971. Patent 3,833,005 was issued and is substantially identical to the "Third Prototype" drawings of May 27, 1970.

In the Wingrove design, the external transmitter sends a predetermined number of RF pulses to the implanted unit. Wingrove chose the parameters of the time frame within which the pulses had to be received with the aim of preventing noise frequencies encountered in nature from meeting the conditions. Thus the RF pulses had to persist for longer than 11 milliseconds, but not more than 14 milliseconds. The lower time threshold is established in resistor 22 and capacitor 26 in decoder 20 as found in Figure 1 of the Wingrove patent. The higher time threshold is determined by resistor 31 and capacitor 27. If the proper RF pulses are received, NOR gate 29 is activated, allowing counter 40 to be reset. Counter 40 which corresponds to the Terry counter 43 determines the rate at which stimulating pulses will be emitted implantable pulse generator 100.

While decoder 20, which functions as the safety circuit, is not a counter, it operates in much the same manner. In order for the RF pulses to persist for the required length of time, it is necessary that the implanted unit receive a predetermined number of RF pulses. The use of RF pulses of a predetermined width in order to enable counter 40 to be reset is substantially equivalent to the use of digital counter 31 in the Terry Patent. The difference between these are such that they would be obvious to one with ordinary skill in the art.

Mr. Prohovsky compared the Terry claims with the prior Wingrove work. He testified that Wingrove anticipates all nine claims of the Terry patent. We conclude that the Wingrove work does in fact anticipate the claims in the Terry Patent.

Obviousness

Even had the Terry Patent claims not been anticipated within the meaning of 35 U.S.C. § 102(g), we find that the differences between the prior art and the subject matter of the Terry Patent as a whole would have been clearly obvious to one with ordinary skill in the art of electrical engineering.

In reaching this conclusion, we have considered the scope and content of the prior art, including the Lozin Patent, the Telestimulator, the prior Wingrove work, and the Chardack, Bowers and Keller Patents. Prior reductions to practice under 35 U.S.C. § 102(g) are properly considered in making a determination of obviousness under 35 U.S.C. § 103. *Sutter Products Co.* v. *Pettibone Mulliken Corp.*, 428 F.2d 639 (7th Cir. 1970).

The Lopin Patent, the Telestimulator, and the Wingrove work are discussed above.

United States Patent No. 3,198,195, issued to Chardack, was filed on October 18, 1962. It claims an invasive needlelike device for changing the operating parameters of a pacer after implantation.

United States Patent No. 3,311,111, issued to Bowers, filed on August 11, 1964, and assigned to General Electric, discloses a controllable electric body tissue stimulator incorporating bistable switches, such as magnetic reed switches that may be actuated by an auxiliary magnetic field applied externally to the body. The reed switches are used to externally adjust the operation of the device.

The Keller Patent discloses a digitally timed pacer using a clock source and a frequency dividing chain to achieve timing.

The need for a safety circuit when using externally programmable implantable devices is elementary. The work of Lenzkes and Wingrove demonstrate the obviousness of the solution to the problem of inadvertent reprogramming. The differences in the prior art between the designs and means of preventing such inadvertent reprogramming are insubstantial. Because of the clear obviousness to the person of ordinary skill of the differences between the subject matter claimed by the Terry patent and the prior art, we need not consider secondary factors such as long felt need, commercial success, and the like. *See Cathodic Protection Service* v. *American Smelting & Refining Company*, 594 F.2d at 513; *Centsable Products, Inc.* v. *Lemelson*, 591 F.2d 400, 403-04 (7th Cir. 1979).

Based on all of the above findings with reference to the Lopin Patent, the Telestimulator, the Wingrove work, and the Chardack, Bowers, and Keller Patents, we conclude that the differences between the Terry Patent and the prior art would have been obvious to one with ordinary skill in the art.

Accordingly, we declare that Terry Patent 3,805,796 is invalid, and that said patent is not infringed by plaintiff because of the making, selling, or using of any apparatus made, sold or used by plaintiff. Plaintiff's claim for attorney's fees and costs is DENIED.

Let judgment be entered accordingly.

Dated: August 31, 1981.

(s) EDWARD J. DEVITT
EDWARD J. DEVITT, *Senior Judge*
United States District Court

35 U.S.C. 102

"A person shall be entitled to a patent unless—

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or

(c) he has abandoned the invention, or

(d) the invention was first patented or caused to be patented by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application filed more than twelve months before the filing of the application in the United States, or

(e) the invention was described in a patent granted on an application for patent by another filed in the United states before the invention thereof by the applicant for patent, or

(f) he did not himself invent the subject matter sought to be patented, or

(g) before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce the practice, from a time prior to conception by the other."

35 U.S.C. 103

Conditions for patentability; non-obviousness subject matter.

"A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made."

United States Patent [19]

Terry, Jr. et al.

[11] **3,805,796**

[45] **Apr. 23, 1974**

[54] IMPLANTABLE CARDIAC PACER HAVING ADJUSTABLE OPERATING PARAMETERS

[75] Inventors: **Reese S. Terry, Jr.**, Miami; **Gomer L. Davies**, Fort Lauderdale, both of Fla.

[73] Assignee: **Cordis Corporation**, Miami, Fla.

[22] Filed: **Jan. 22, 1973**

[21] Appl. No.: **325,334**

Related U.S. Application Data

[63] Continuation of Ser. No. 141,694, May 10, 1971, abandoned.

[52] **U.S. Cl.** ..... **128/419 P**, 128/421

[51] **Int. Cl.** **A61n 1/36**

[58] **Field of Search** ..... 128/419 C, 419 B, 419 E, 128/419 P, 419 R, 422, 423

[56] **References Cited**

UNITED STATES PATENTS

3,631,860	1/1972	Lopin	128/419 P
3,311,111	3/1967	Bowers	128/419 P

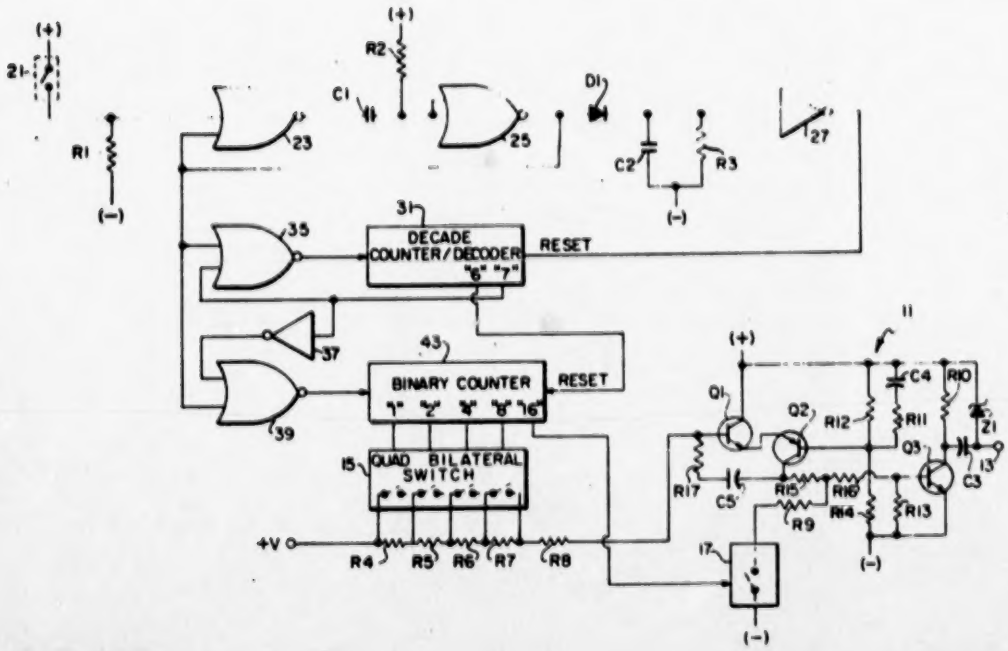
Primary Examiner—William E. Kamm

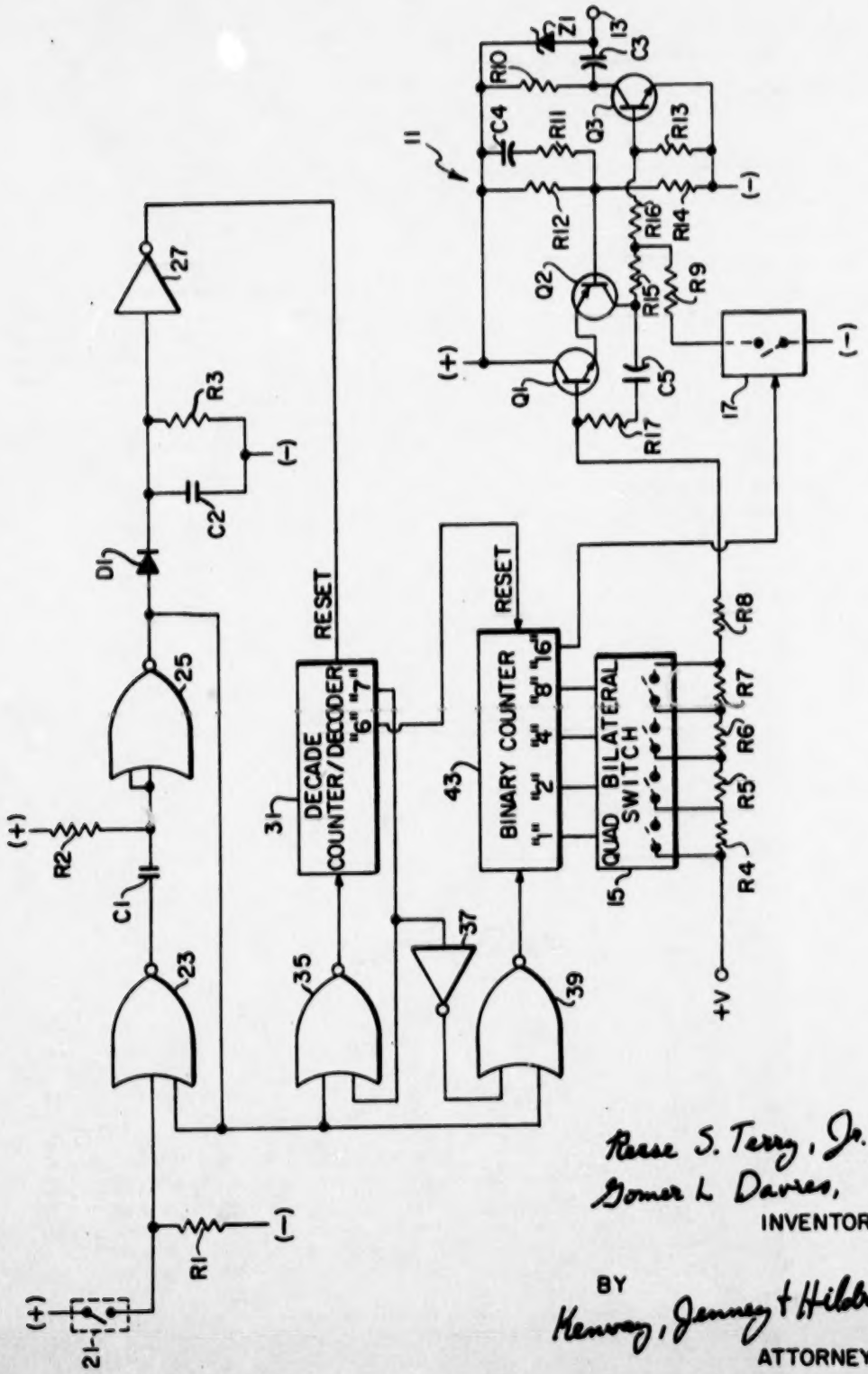
Attorney, Agent, or Firm—Kenway, Jenney & Hildreth

[57] **ABSTRACT**

In the implantable cardiac pacer disclosed herein, various operating parameters are determined or controlled by the information held in a digital storage register such as a binary counter. The information so held may be varied by means of pulse signals transmitted through the body of a patient within whom the pacer is implanted. Rate-sensing and count threshold control circuits are provided to prevent unintended changes in operating parameters.

9 Claims, 1 Drawing Figure





Reese S. Terry, Jr. and
Homer L. Davies,
INVENTORS

BY
Kenway, Jenney & Hildreth
ATTORNEYS

IMPLANTABLE CARDIAC PACER HAVING ADJUSTABLE OPERATING PARAMETERS

This is a continuation of application Ser. No. 141,694 filed May 10, 1971, now abondoned.

BACKGROUND OF THE INVENTION

This invention relates to fully implantable prosthetic or therapeutic devices and more particularly to cardiac pacers in which various operating parameters may be adjusted or varied without surgically obtaining access to the pacer itself.

Various means have been proposed for altering the operating parameters of an implanted cardiac pacer without requiring surgery as such. For example, it has been proposed to utilize needle-like adjusting tools to select resistance values and to use bistable magnetic reed switches for performing various switching functions. However, each of these prior art adjustment means has heretofore typically been rather limited in application. A serious drawback in most of these prior art systems is that the range of adjustment or the number of adjustments which can be made is highly limited. Further, there may be a problem in retaining the desired value after the adjustment procedure per se is complete. In the case of bistable magnetic reed switches, transient magnetic fields may cause the switch to reverse state. The switch will then remain in that state indefinitely and thereby cause an undesired mode of operation. In the case of needle-like adjusting tools, the danger of infection due to penetrating the patient's epidermis remains even though that danger is reduced by the needle-like character of the tool.

Among the several objects of the present invention may be noted that provision of apparatus which permits the adjustment or variation of several operating parameters of an implanted prosthetic device such as a cardiac pacer without requiring surgical access to the device; the provision of such apparatus in which a parameter may be adjusted over a wide range and to any one of a wide variety of preselected values within the range; the provision of such apparatus in which predetermined combinations of different operating parameters may be selected simultaneously; the provision of such a system which provides for the reliable storage of the parameter-determining information; the provision of such apparatus which is relatively immune to electrical noise and transient magnetic fields; and the provision of such apparatus which is highly reliable and which is relatively simple and inexpensive. Other objects and features will be in part apparent and in part pointed out hereinafter.

SUMMARY OF THE INVENTION

Briefly, an implantable pacer constructed in accordance with the present invention employs means for detecting pulse signals having predetermined characteristics which are applied externally of a patient within whom the pacer is implanted. A counter is interconnected with the detecting means and is advanced by the detected pulse signals. A cardiac stimulation pulse generator is provided in which at least one output parameter is adjustable. Decoding means are interconnected between the counter and the pulse generator for setting the adjustable parameter to a value corresponding to the particular count accumulated by the counter. Accordingly, the output parameter may be adjusted by means of pulse signals applied externally of the patient.

BRIEF DESCRIPTION OF THE DRAWING

The single drawing is a schematic block diagram of an implantable cardiac pacer having operating parameters which are adjustable in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawing, an essentially conventional cardiac stimulation pulse-generating circuit is indicated generally at 11. Appropriate supply potentials are provided as indicated. An NPN transistor Q1 and a PNP transistor Q2 are interconnected in a so-called complementary-symmetry type of relaxation oscillator. The voltage at the base terminal of PNP transistor Q2 is controlled by a voltage divider comprising resistors R12 and R14, this voltage being filtered by a capacitor C4 with the filter source impedance being determined by a resistor R11.

The collector of transistor Q2 is connected to the base of transistor Q1 through a capacitor C5 and a resistor R17 connected in series therewith. As will be understood by those skilled in the art, this connection provides regenerative feedback during the pulse output portion of the oscillator's cycle of operation. The oscillator output signal, taken from the collector of transistor Q2, is applied, through a pair of resistors R15 and R16, to the base terminal of an NPN output transistor Q3. This transistor is normally biased off by means of a resistor R13. The collector terminal of output transistor Q3 is provided with a load resistor R10 and is coupled, through a capacitor C3, to the pacer output terminal 13. As is understood, the output terminal 13 will be coupled to a patient's cardiac tissue through an appropriate lead system, as is conventional. The lead system also establishes a common ground potential. The output circuit is protected by a zener diode Z1 in conventional manner.

As is understood, the repetition rate of the complementary symmetry oscillator depends upon the bias current provided to the base terminal of transistor Q1. This current serves to re-charge the capacitor 5 between output pulses. This bias current is provided from the positive supply voltage through a series of timing resistors R4–R8 which are graded in value according to a predetermined sequence. Selected ones of the resistors R4–R8 may be shunted by the operation of a quadbilateral switch 15. As will be understood by those skilled in the use of integrated circuits in digital applications, the quadbilateral switch 15 will typically comprise a plurality of active semiconductor elements formed in a single semiconducting wafer or chip. However, for the purpose of facilitating the description of the present invention, the switching function performed by this circuitry is conveniently represented in the drawing by four conventional switch symbols. Each such switch is under the control of a respective input signal, as indicated. As will be understood, 16 values of total series resistance may be obtained by closing the individual switches in various combinations. Correspondingly, 16 different pulse repetition rates will be available from the oscillator comprising transistors Q1 and Q2.

The junction between resistors R15 and R16 can selectively be shunted to ground through a resistor R9 and a semiconductor switch or gate 17. Again, this function is indicated by a conventional switch symbol although semiconductor switching elements are preferred in actual practice. The operation of the switch is under the control of a respective input signal, as indicated. When the gate or switch 17 is closed, a portion of the drive or output current from the oscillator transistors Q1 and Q2 is shunted away from the base circuit of the output transistor Q3 through resistor R9. The stimulation pulse output current is correspondingly reduced. Thus, the gate 17 provides a means for selecting between two output current levels. In other words, means are provided for adjusting the value of a second operating parameter of the stimulation pulse generating circuitry. Since the number of available states double with each further stage added to the binary counter, it can be seen that the number of combinations of several different parameters may easily be expanded. For example, selected count bits may be used to control whether the pacer operates in a synchronous or non-synchronous mode or in a standby or continuous mode.

In accordance with the present invention, the pulse repetition rate and the output current of this stimulation pulse generator 11 may be adjusted or controlled while the pacer is implanted, without surgically entering the patient's body. In the embodiment illustrated, pulse signals for transmitting the information used in determining these output parameters is transmitted into the patient's body by means of a magnetic field which is sensed by a magnetic reed switch 21. Reed switch 21 is interconnected with the positive supply so as to provide a source of input pulses to one of the input terminals of a NOR gate 23. This input terminal is normally biased negatively through a resistor R1. The output signal from NOR gate 23 is coupled, through a capacitor C1, to both input terminals of a second NOR gate 25, which thus functions as an inverter. These input terminals are normally biased in the positive sense through a resistor R2. The output signal from NOR gate 25 is, in turn, applied back to the other input terminal of the first NOR gate 23.

As will be understood by those skilled in the art, this interconnection of the NOR gates 23 and 25 provides the mode of operation of a one-shot multivibrator. The time constant or period of the multivibrator is determined by the relative values of capacitor C1 and resistor R2 and is selected so as to provide, for each triggering pulse, a square-wave output pulse of longer duration than any contact bounce which might be expected from the magnetic reed switch 21. This operation thus provides a pulse shaping so that the resultant electrical pulse signals are suitable for use with digital circuitry in conventional manner.

While magnetic pulse signals are presently preferred as a method of communicating information to the implanted device, other types of signals, appropriately selected to avoid interference from ambient interference, may also be used. For example, bursts of acoustic energy at preselected frequency can be transmitted through tissue and detected. Likewise, bursts of electromagnetic energy at relatively low r.f. frequencies can be detected and used to advance the counters or registers of the present invention. Relatively low r.f. frequencies, e.g., 15–150 kHz, have the advantage that they can penetrate a shield around the implanted device which would protect the circuitry from high frequency transients which might affect the logic circuitry.

The pulse signals obtained from the multivibrator are applied, through a diode D1, to a timing capacitor C2 which is shunted by a resistor R3. The voltage on capacitor C2 is, in turn, applied to an inverting gate 27. Gate 27 functions essentially as a voltage threshold device, the output signal from gate 27 being positive or a digital "one," except when the voltage on capacitor C2 is above a predetermined voltage level or threshold which is the level of actuation of the gate. Together with the capacitor C2 and resistor R3, gate 27 thus operates as a rate detector. When pulses from the one-shot multivibrator are applied through diode D1 to capacitor C2 so as to re-charge that capacitor faster than it is discharged by the resistor R3, the output signal from gate 27 will remain negative so as to constitute a logic "zero."

The output signal from gate 27 is applied as a reset signal to a decade counter 31. Decade counter 31 is assumed to be of the integrated digital circuit type having an integral decoder so that separate output signals corresponding respectively to each of the ten successive states of the counter are available without external matrixing. In the embodiment illustrated, only the "6" and "7" output signals are utilized.

The shaped input pulses obtained from the one-shot multivibrator are applied to the input terminal of counter 31, through a NOR gate 35. The "7" output signal from the decade counter 31 is applied as a second input to NOR gate 35 so as to selectively control the application of these input pulses. As will be understood, this connection will allow the counter to count up to its seventh state. At this point, the "7" output signal becomes a digital "one." Accordingly, the output signal from gate 35 will be held at a digital "zero" and further counting is prevented.

The "7" signal from the decade counter 31 is also applied, through an inverting gate 37, to a NOR gate 39. NOR gate 39 is connected so as to control the application of the input pulses, obtained from the one-shot multivibrator, to a binary counter 43. Since the "7" signal from the decade counter 31 is inverted prior to its application to the NOR gate 39, it will be seen that the binary counter 43 is inhibited from counting until the decade counter 31 reaches its seventh state. The "6" output signal from the decade counter 31 is applied as the reset signal to the binary counter 43.

Thus, when the decade counter 31 passes through its sixth state, the binary counter 43 will be reset. Then, when the decimal counter 31 reaches its seventh state, it will stop counting and the binary counter 43 will begin to count upwards from its reset or "zero" state in response to any pulse input signals applied thereto by the multivibrator circuit.

Counter 43 is a five-stage binary counter, an output signal being provided from each stage. The output signals from the first four stages, i.e., the "1," "2," "4" and "8" signals, are applied to control the quad-bilateral switch 15. Thus, the value of the repetition rate-controlling resistance will be a function of the count held by the first four stages of binary counter 43. The "16" output signal from binary counter 43, i.e., the signal from the fifth stage, controls the gate 17 which, as noted previously, affects the output current level of

the stimulation pulse-generating circuit **11**. The counter **43** has 32 possible states, 16 in which the "16" signal is a logic "one" and 16 in which that signal is a logic "zero." Accordingly, it will be seen that any of the 16 different pulse repetition rates can be provided at either of the two output current levels. In other words, there are 32 output parameter combinations which can be applied to the stimulation pulse generator **11** and the selection of which of these 32 exists at any one time is under the control of the count accumulated in the binary counter **43**.

Summary of Operation

Briefly then, the operation of the embodiment illustrated is as follows. The output parameters of the stimulation pulse generator **11** are determined in correspondence with the count held in the binary counter **43**. The existing parameter values persist until the counter **43** is set to some different value. Pulse signals for changing the count held in counter **43** are introduced by applying, through the patient's body, bursts or trains of magnetic pulses which will actuate the magnetic reed switch **21**. Each operation of the reed switch triggers the one-shot multivibrator comprising gates **23** and **25** so that a squarewave pulse, suitable for use with digital circuitry, is generated. If successive pulses follow at a rate which is within the time constant determined by capacitor **C2** and resistor **R3**, the gate **27** resets the counter **31** and this counter begins to count the shaped input pulses. After the counter **31** receives six of the succeeding pulses, the binary counter **43** is reset. When the decade counter reaches its seventh state, it is stopped from further counting and subsequent shaped input pulses are applied to the binary counter **43** so that this counter is then advanced from its initial or all "zero" state. The total length of the pulse train is selected so that the new count introduced into the binary counter **43** corresponds to that state of the counter which will produce the desired output parameters, i.e., through the quadbilateral switch **15** and the gate **17**. For example, if it is desired to set the stimulation pulse generator output parameters to values corresponding to the seventh state of the binary counter **43**, the applied pulse train should produce fifteen actuations of the magnetic reed switch **21**. The first actuation causes the gate **27** to release the reset signal from the counter **31**, the next seven counts advance the decade counter **31** and the last seven counts advance the binary counter **43** to the desired state. Since magnetic reed switches can operate at frequencies of several hundred Hz and the digital counting circuitry will operate much faster, a complete resetting cycle can be accomplished in less than a typical heartbeat period. If even faster parameter resetting is sought, semiconductor magnetic or electric sensing devices may be used.

In addition to providing timed resetting of the output control counter **43**, the count threshold established by the decade counter **31** also provides the additional desirable function of establishing a count threshold which must be exceeded before any change in output parameter will be effected. Thus, a short burst of electrical noise pulses which might find their way into the circuitry at the proper repetition rate to actuate the rate-sensitive circuitry, still would not typically advance the counter **31** sufficiently far to erase the output parameter information previously stored in the binary counter **43**. Accordingly, a very high degree of noise immunity is provided.

Apparatus in accordance with the embodiment illustrated was constructed using components having the values and/or manufacturer's part designation as given in the following table and this apparatus operated in the manner described.

TABLE

	Ohms
R1	100,000
R2	1,000,000
R3	1,000,000
R4	176,000
R5	232,000
R6	564,000
R7	1,024,000
R8	1,863,000
R9	10,000
R10	27,000
R11	5,600
R12	2,200,000
R13	22,000
R14	3,300,000
R15	10,000
R16	10,000
R17	1,000
	Microfarads
C1	0.0047
C2	0.047
C3	4.7
C4	0.1
C5	0.22
NOR Gates 23, 25, 35 and 39	RCA CD 4001
Decade Counter	RCA CD 4017
Binary Counter	RCA CD 4004
Quad Bilateral Switch	RCA CD 4016
Gates 27, 37 and 17	RCA CD 4007

With regard to the inverting gates **27** and **37**, it may be noted that these gates, in the RCA integrated circuit designated, are in fact pairs of separable field-effect transistors on the same chip and a remaining one of the transistors on the same integrated circuit chip is employed as the switching gate **17**. While this particular embodiment was made up using commercially available integrated circuit devices, it should be understood that essentially the same circuitry can be formed as a single special purpose integrated circuit using so-called large scale integrated circuit (LSI) techniques, as can other embodiments falling within the scope of the appended claims. The particular integrated circuits designated are of the complementary MOSFET (metal oxide semiconductor, field-effect transistor) type. An advantage of this type of circuitry in implantable stimulation devices is that the logic gates employed draw very little current except in actual switching and thus average current drain is very low.

While the parameter-controlling apparatus of the present invention has been illustrated in conjunction with stimulation pulse generating circuitry using analog timing and output current control, it should be understood that, the functional parameters of other types of stimulation pulse-generating circuitry may also be controlled in accordance with the count held in a digital storage register such as the binary counter **43**. For example, apparatus of the present invention might also be used in conjunction with a digitally timed implantable cardiac pacer, e.g., of the type disclosed in U.S. Pat. No. 3,557,796 Keller et al. Similarly, the operating parameters of other types of tissue stimulators, e.g., bladder, phrenic nerve, or carotid sinus, may also be controlled in accordance with the present invention.

In view of the foregoing, it may be seen that several objects of the present invention are achieved and other advantageous results have been attained.

As various changes could be made in the above constructions without departing from the scope of the invention, it should be understood that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

What is claimed is:

1. An implantable cardiac pacer comprising:
means for detecting pulse signals having predetermined characteristics, which pulse signals can be applied externally of a patient within whom said pacer is adapted to be implanted;
a first counter interconnected with said detecting means for selectively counting detected pulse signals;
a second counter, controlled by said first counter and also responsive to said pulse signal detecting means for counting detected pulse signals occurring after the count held by said first counter reaches a preselected threshold value;
a cardiac stimulation pulse generator having at least one changeable output parameter; and
decoding means interconnected with said second counter for controlling said output parameter in predetermined correspondence with the value of the count held by said second counter.

2. In a fully implantable therapeutic device providing an electrically controlled physiological function, apparatus for adjusting the operating parameters of the device while implanted, said apparatus comprising:
means for detecting pulse signals having predetermined characteristics, which pulse signals can be applied externally of a patient within whom said device is adapted to be implanted;
a first counter interconnected with said detecting means for selectively counting detected pulse signals;
a second counter, controlled by said first counter and also responsive to said pulse signal detecting means for counting detected pulse signals occurring after the count held by said first counter reaches a preselected threshold value;
decoding means interconnecting with said second counter for controlling operating parameters of said device in accordance with the count held by said second counter; and
means for resetting said first counter if no pulse signals are received for a predetermined period.

3. In a fully implantable device for automatically providing an electrically controlled physiological function, apparatus for adjusting the operating parameters of the device while the device is implanted, said apparatus comprising:
a magnetically operable switch for detecting magnetic pulse signals, which pulse signals can be applied externally of a patient within whom said device is adapted to be implanted;
a first counter interconnected with said switch for selectively counting operations of said switch;
means for resetting said first counter if no pulse signals are received for a preselected period;
a second counter, controlled by said first counter and selectively responsive to the operation of said switch;
means controlled by said first counter for resetting said second counter when the count held by said first counter reaches a preselected threshold level and for subsequently enabling said second counter to count switch operations; and
decoding means interconnected with said second counter for controlling the operating parameters of said device in accordance with the count held by said second counter.

4. A device as set forth in claim 3 including a one-shot multivibrator which is triggered by the operation of said switch and which generates square-wave output pulses of predetermined duration, said counters being responsive to the multivibrator output pulse to count operations of said switch.

5. A device as set forth in claim 3 wherein said first and second counters comprise complementary MOS-FET integrated logic circuits.

6. An implantable cardiac pacer comprising:
a magnetically operable switch for detecting magnetic pulse signals, which pulse signals can be applied externally of a patient within whom said pacer is adapted to be implanted;
a first counter interconnected with said switch for selectively counting operations of said switch;
means for resetting said first counter if no pulse signals are received for a preselected period;
a second counter, controlled by said first counter and selectively responsive to the operation of said switch;
means controlled by said first counter for resetting said second counter when the count held by said first counter reaches a preselected threshold level and for subsequently enabling said second counter to count switch operations;
a cardiac stimulation pulse generator having at least one adjustable output parameter; and
means interconnected with said second counter for setting said output parameter to a value corresponding to the count held by said second counter.

7. In a fully implantable device for providing an electrically controlled physiological function, apparatus for adjusting the operating parameters of the device while the device is implanted, said apparatus comprising:
means for detecting pulse signals having predetermined characteristics, which pulse signals can be applied externally of a patient within whom said device is adapted to be implanted;
means responsive to a first predetermined grouping of detected pulse signals for providing a control signal;
a parameter control register having a multiplicity of states;
means for controlling the operating parameters of said device in accordance with the existing state of said control register; and
means responsive to said control signal for changing the state of said register in accordance with predetermined groupings of detected pulse signals following said first grouping of pulse signals, thereby to vary the operating parameters of said device.

8. In a fully implantable device for automatically providing electrical stimulation of tissue, apparatus for adjusting the operating parameters of the device while the device is implanted, said apparatus comprising:

means for detecting pulse signals having predetermined characteristics, which pulse signals can be applied externally of a patient within whom said device is adapted to be implanted;

means including a counter responsive to a first predetermined sequence of detected pulse signals for providing a control signal;

a parameter control counter having a multiplicity of sequential states;

means for controlling the operating parameters of said device in accordance with the existing state of said control counter; and

means enabled by said control signal for advancing the state of said control counter in response to detected pulse signals following said first sequence of pulse signals, thereby to vary the operating parameters of said device.

9. Apparatus as set forth in claim 8 wherein said control counter is responsive to said control signal and is reset thereby to a preselected state.

* * * * *

United States Patent [19]

Lenzkes

[11] **3,727,616**

[45] **Apr. 17, 1973**

[54] **ELECTRONIC SYSTEM FOR THE STIMULATION OF BIOLOGICAL SYSTEMS**

[75] Inventor: **Herbert H. Lenzkes, Pomona, Calif.**

[73] Assignee: **General Dynamics Corporation, Pomona, Calif.**

[22] Filed: **June 15, 1971**

[21] Appl. No.: **153,316**

[52] U.S. Cl. ..... **128/422, 128/419 E**

[51] Int. Cl. **A61n 1/36**

[58] Field of Search ..... **128/419 C, 419 E, 128/419 P, 419 R, 420, 421, 422, 423, 2.1 A; 340/184**

[56] **References Cited**

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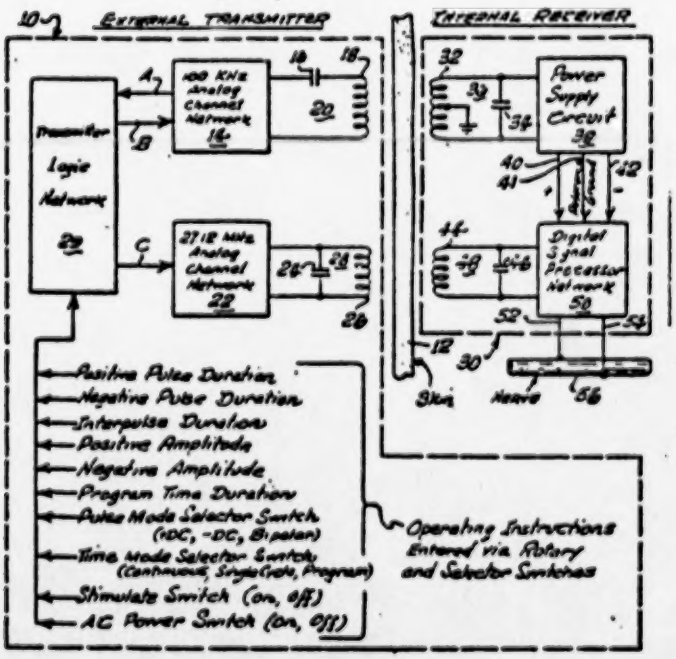
Primary Examiner—William E. Kamm
Attorney—Edward B. Johnson

[57] **ABSTRACT**

A receiver totally implanted within a living body is inductively coupled by two associated receiving coils to a physically unattached external transmitter which transmits two signals of different frequencies to the receiver via two associated transmitting coils. One of the signals from the transmitter provides the implanted receiver with precise control or stimulating signals which are demodulated and processed in a signal processor network in the receiver and then used by the body for stimulation of a nerve, for example, while the other signal provides the receiver with a continuous wave power signal which is rectified in the receiver to provide a source of electrical operating power for the receiver circuitry without need for an implanted battery.

9 Claims, 13 Drawing Figures



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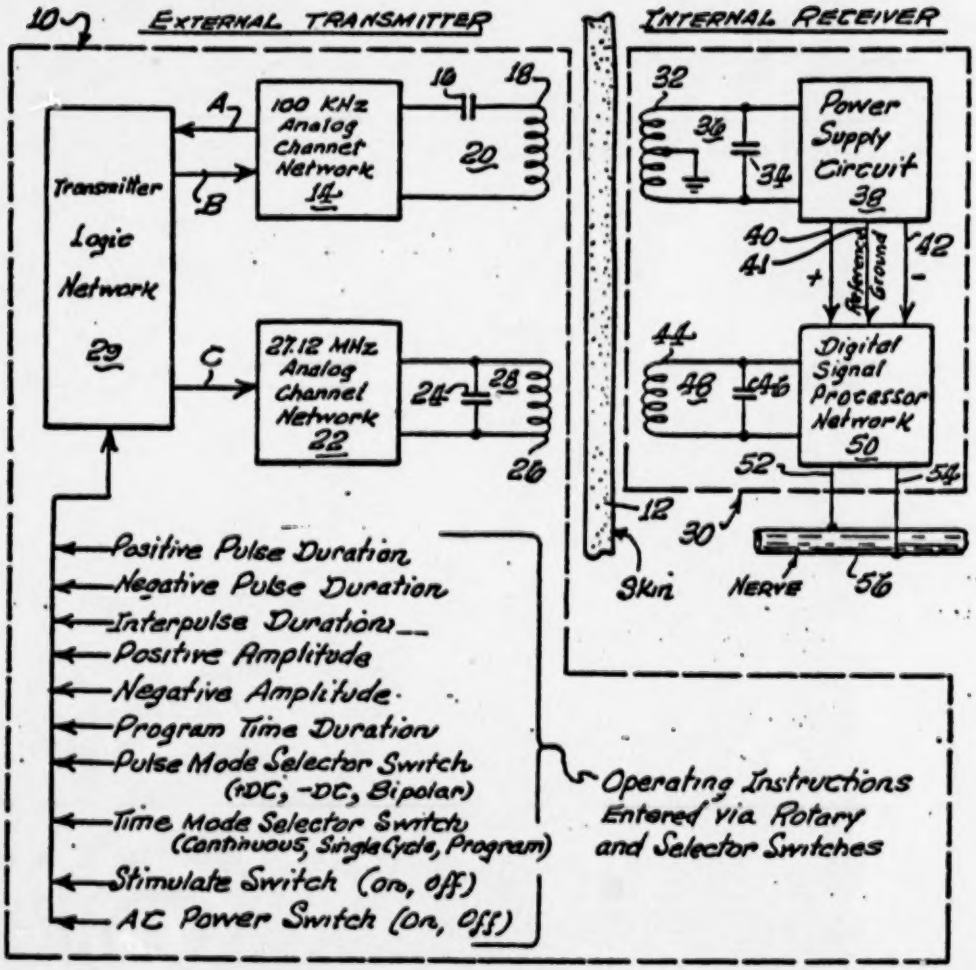
SHEET 1 OF 5

FIG. 1.



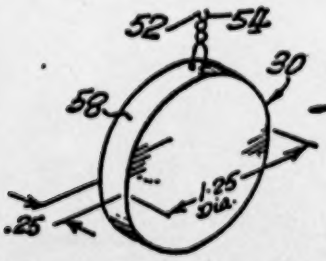


FIG. 2.

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FIG. 3.

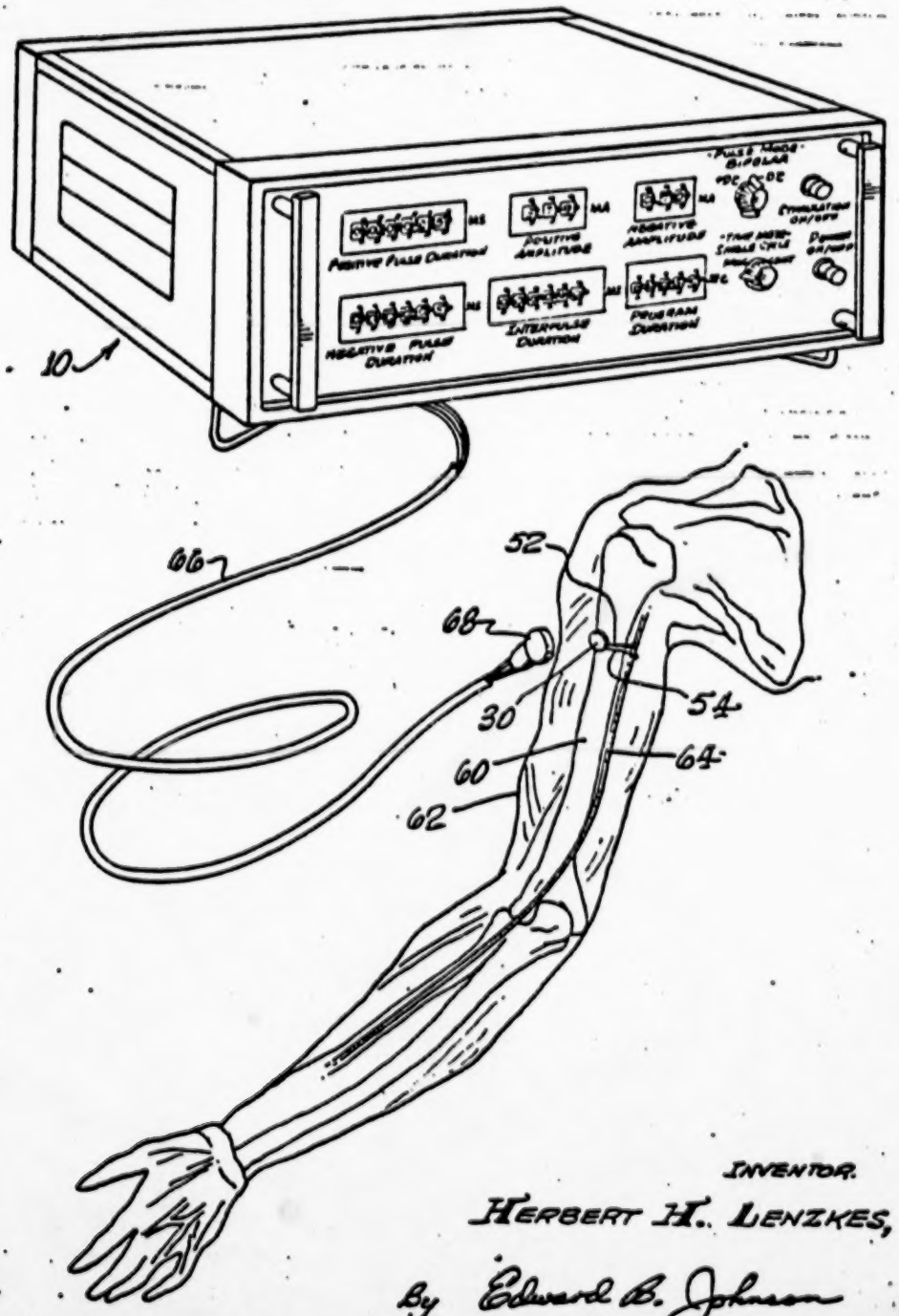

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FIG. 4.

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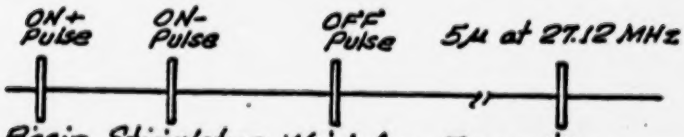

FIG. 5(a) Basic Stimulation Word from Transmitter

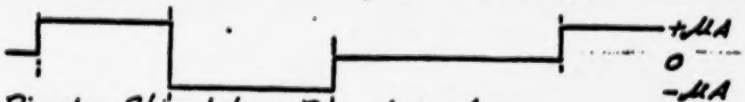

FIG. 5(b) Bipolar Stimulating Current to Nerve

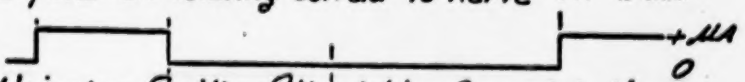

FIG. 5(c) Unipolar Positive Stimulating Current to Nerve

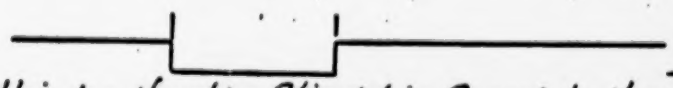

FIG. 5(d) Unipolar Negative Stimulating Current to Nerve

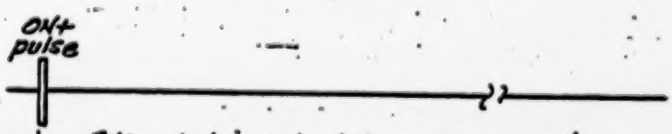

FIG. 5(e) +DC Stimulation Word from Transmitter

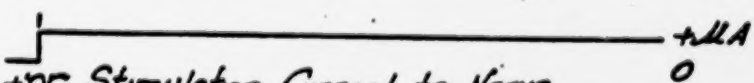

FIG. 5(f) +DC Stimulation Current to Nerve

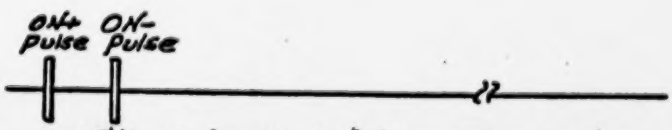

FIG. 5(g) -DC Stimulation Word from Transmitter

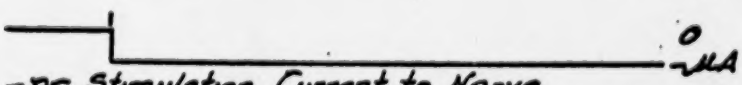

FIG. 5(h) -DC Stimulation Current to Nerve

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FIG. 6.

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ELECTRONIC SYSTEM FOR THE STIMULATION OF BIOLOGICAL SYSTEMS

BACKGROUND OF THE INVENTION

This invention is directed to means for providing a precisely controlled bipolar current pulse of given polarity, magnitude and duration to a living body for controlling pain, permitting movement of paralyzed extremities, controlling spasticity, stimulating paralyzed urinary bladders and preventing atrophy in clinical applications and for functional and behavioral changes in neurophysiological applications, for example. The system of the invention utilizes a pulse position modulation technique for electrically stimulating biological systems such as nerves, for example, in a manner which presently does not exist. The resulting stimulation output is a constant current biphasic or monophasic signal. Because of the digital nature of the inventive system, accurate and reliable current stimulating levels are achieved with fast rise and fall times. Safety features have been included in the system to prevent extraneous stimulation due to interfering signals. When the implanted receiver is not activated by the external transmitter, any extraneous signals are shunted by a low impedance path in the receiver.

The inventive system is essentially digital in nature, whereas known systems in the prior art employ analog techniques. In addition, the prior art systems employ pulse width modulation in which the resulting pulsed radio frequency signal is detected and filtered to obtain a stimulation waveform. This prior art method, while simple in nature, has many limitations. For example, it cannot provide a precisely controlled amplitude because of its dependency on the coupling coefficient between a primary tuned circuit and a secondary tuned circuit, it cannot provide a biphasic stimulation waveform nor can it generate a direct current stimulation. In addition, its unipolar pulses are not rectangular because an exponential discharge circuit is normally employed. Stimulators of the prior art are designed for specific applications and lack the parameter versatility and safety that can be achieved with the inventive system.

SUMMARY OF THE INVENTION

The system of the present invention includes a transmitter that is inductively coupled by two transmitting coils to a receiver located totally within a living body. The system of the present invention is sometimes called a "Biostimulator" and at other times a "Telestimulator". The transmitter, which is located outside the body, transmits two signals of different frequencies to the receiver via the two transmitting coils. The dual frequency link of the system provides the implanted receiver with control signals or operating information and also a signal from which the receiver can extract its electrical operating power. The receiver basically comprises two receiving coils, a signal processor and a power supply. The output of the receiver is coupled to two electrodes via very small electrical wires which may be attached to a nerve, for example, to stimulate the nerve or to block it. The desired stimulating pulse characteristics such as amplitudes, width, interpulse, periods, etc., are initially entered into the control panel of the transmitter via suitable switches such as rotary thumbwheel switches, for example. These data are converted to a digital format part of which is transmitted to the receiver as a 21-bit Amplitude Data Word. This information is received, decoded and stored by the signal processor portion of the receiver to provide the proper amplitude reference to stimulate the nerve. The remaining portion of the data which has been previously entered into the transmitter is sent to the receiver as a series of Stimulation Words. Each of the Stimulation Words comprises three 5-microsecond radio frequency (r-f) pulses at substantially 27.12 MHz. The time spacing between the pulses determines the time duration of the various parts of the stimulating waveform. Each word operates in real-time to alternately stimulate the nerve with a positive amplitude, a negative amplitude and a zero amplitude. The transmitter also provides a substantially 100 KHz continuous wave power signal which is inductively coupled into the power supply coil in the receiver and rectified to provide electrical power for the receiver circuitry. The power signal is always present whenever the sytem is in use.

Therefore, it is an object of this invention to provide an electronic system for the stimulation of biological systems in a living body in the form of an implantable receiver capable of providing proper stimulation when used in conjunction with an external transmitter.

Another object of this invention is to provide an electronic system for the stimulation of biological systems in a living body in which no internal batteries are utilized nor any direct wire connections into the body are made.

It is a further object of this invention to provide a stimulator system for a living body wherein a dual frequency external transmitter provides inductively coupled control and power signals to a compatible receiver located within the living body.

Other objects and features of the invention, as well as the many advantages thereof, will be readily apparent to those skilled in the art from a consideration of the following written description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified functional block diagram illustrating the overall system involved in the present invention.

FIG. 2 is a dimensioned view of an encapsulated embodiment of the implantable receiver of the system.

FIG. 3 is a diagrammatic showing of the receiver of FIG. 2 implanted in an arm and an embodiment of an associated transmitter.

FIG. 4 is a functional block diagram of the transmitter shown in FIG. 3.

FIGS. 5*a*–5*h* show electrical waveforms available from the transmitter as stimulation words and the resulting stimulating currents.

FIG. 6 is a functional block diagram of the receiver shown in FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings, and more particularly to FIG. 1, there is shown a simplified functional block diagram of the overall system which includes a transmitter 10, which may be of the laboratory type, for ex-

ample, externally located with respect to the outer surface of a skin portion 12 of a living body (not shown). Stimulating and operational information data for operation of the transmitter 10 are listed in FIG. 1. A 100 KHz analog channel network 14 in transmitter 10 provides a substantially 100 KHz continuous wave power signal to a capacitor 16 and a coil or inductor 18 which comprise a substantially 100 KHz series resonant circuit 20. The coil 18 acts as a transmitting antenna. A 27.12 MHz analog channel network 22 in transmitter 10 provides pulsed radio frequency data at substantially 27.12 MHz to a capacitor 24 and a coil or inductor 26 which comprise a substantially 27.12 MHz parallel resonant circuit 28. The coil 26 acts as a transmitting antenna. Coupled to the 100 KHz analog channel network 14 and to the 27.12 MHz analog channel network 22 by connecting leads A, B and C is a transmitter logic network 29 which processes the stimulating and operational information data listed in FIG. 1.

In practice, the capacitor 16 in the resonant circuit 20 (being relatively large in size) is physically located with the other components of the 100 KHz analog channel network 14, whereas the inductor 18 of the resonant circuit 28 together with the inductor 26 and capacitor 24 of the resonant circuit 28 are encased in a suitable protective housing and as a unit, the combination is sometimes called "the transmitter probe". Each of the circuits encased in the "probe" is preferably connected to its respective channel by a coaxial cable (not shown).

As a point of interest, the simple resonant circuit 28 could be changed, if desired, to a preloaded, tapped resonant circuit wherein a resistor is connected in parallel with the inductor 26 and two series capacitors are connected in parallel with the resistor/inductor combination. The center conductor of the appropriate coaxial cable would be connected between the two series capacitors.

The particular frequencies chosen for the preferred embodiment are by way of example only, and it is well understood by those skilled in the art that other frequency combinations as authorized by FCC regulations may be substituted.

Positioned completely underneath the skin portion 12 is an implantable receiver 30 which includes a coil or inductor 32 connected in parallel with a capacitor 34 which comprise a 100 KHz parallel resonant circuit 36. The inductor 32 acts as a receiving antenna to receive the inductively coupled 100 KHz power signal from the inductor 18 of the resonant circuit 20. The received power signal is rectified and regulated in a power supply circuit 38 to provide electrical power of the proper potential for the implanted electronics via conductors 40, 42 and the reference ground 41. A coil or inductor 44 is connected in parallel with a capacitor 46 and comprise a 27.12 MHz parallel resonant circuit 48. The coil 44 acts as a receiving antenna to receive the inductively coupled 27.12 MHz control or operating information signal from the coil 26 of the resonant circuit 28. The received control signal is processed in a signal processor network 50 the output of which is connected via male interconnect conductors 52, 54 and very small wires to a nerve 56, for example. In describing the preferred embodiment of the present invention, nerve stimulation has been chosen as one example only of the many uses thereof, and it will be readily understood by those skilled in the art that the present invention can be used in many clinical and neurophysiological applications.

Utilization of microelectronic fabrication techniques during the past few years has resulted in an electronic packaging science wherein many complex electronic circuits can be condensed into small packages. As an illustration of the science of microminiaturization, FIG. 2 shows the dimensions of an actual size example of the receiver 30 of the present invention contained in a 0.25 inch thick circular package of 1.25 inch diameter. This small size allows utilization of the receiver 30 in most parts of the human body. In the example of FIG. 2, the implantable receiver 30 is contained in a hermetically sealed all-ceramic package which is encapsulated with medical-grade silicone rubber 58, for example, to reduce the possibility of body contamination and rejection. The majority of the electronic circuitry is contained on two circular ceramic substrates (not shown). This circuitry generally consists of thick film resistors, chip capacitors, and various semiconductor chips and interconnections. The power supply coil 32 of the receiver 30 is concentrically wound on the outer edge area of a ceramic circular coil form (not shown) which also serves as a housing for the two circular substrates. The signal coil 44 is printed on the outside portion of one of the circular substrates which also acts as a cover for one end of the unit. The male interconnectors 52, 54 are imbedded in the power supply coil form to provide mechanical integrity. The all-ceramic package is extremely rugged and will survive in very adverse environments. The implantable receive 30 is surgically placed within a desired body area as shown in FIG. 3 and is preferably affixed to the nearest bone structure. In FIG. 3, the receiver 30 is affixed to the humerus 60 of an arm 62 by using synthetic materials similar to those used for bone repair, for example, and the receiver output interconnectors 52, 54 are connected to a nerve 64 via very small electrical wires (not shown). In practice, the free ends of two electrical conductors (not shown) having female connectors on the other ends are attached to the nerve to be stimulated. The female connectors are then slipped over the male interconnectors 52 and 54. Also shown in FIG. 3 is an example of the transmitter 10 with its output cabling 66, preferably two coaxial cables, and the encased transmitter "probe" in a housing 68. The transmitter coils 18, 26 in the "probe" housing 68 are wound similarly to receiving coils 32, 44 on a circular coil form or on individual coil forms and are protectively encased or encapsulated in a strong plastic material, for example. Stimulation of the nerve 64 is achieved by placing the transmitter coils 18, 26 contained in the housing 68 approximately, for example, one-half inch near, or actually on, the skin portion closest to the implanted receiver 30 so the receiver coils 32, 44 can easily receive the transmitted signals and then activate the transmitter. The operating instructions listed in FIG. 1 are entered into the transmitter 10 prior to stimulation via suitable switches as shown in FIG. 3 in which actual values are depicted to illustrate an exemplary operational setup. Also shown in the FIG. 3 example of a transmitter are the switches listed in FIG. 1.

Two major problems must be considered in the design and fabrication of devices to be implanted in a living body. These two major problems involve the selection of enclosure and connector materials. The body fluids present a rather formidable challenge to the enclosure or cover for an implantable device because of their corrosive action. Materials that provide long-term protection to the device's electronics and that are compatible with the body chemistry are: ceramic, glass, synthetic resinous materials and some metals such as surgical-grade stainless steel and platinum, for example. The qualities that make an all-ceramic package a highly desirable choice for implantable devices include: mechanical strength, electrical isolation, resistance to body fluids, adequate thermal conductivity, compatibility with hybrid technology and low cost. All connectors must be small and reliable and must also be compatible with the body fluids. The conductors used for the nerve stimulator described herein are made of stainless steel but could also be made of platinum, gold, silver and tantalum or alloys of these metals, for example. Encapsulating materials should be electrically insulating, inert, non-toxic, non-irritating and sterilizable. In addition to the silicone rubber 58, other examples of encapsulant materials are: silastic resins, vinyl chloride, acrylic polymers, polystyrene, tetrafluoroethylene polymers and the like.

Referring now to FIG. 4, there is shown a functional block diagram of the transmitter 10. The stimulating word(s) and operational information data shown in FIG. 1 are again included in FIG. 4. The analog portion of the transmitter consists of two channels, one at 100 KHz and the other at 27.12 MHz, which are functionally identical. The 27.12 MHz analog channel network 22 comprises an oscillator 70 connected through a series switch 72 to a power amplifier 74. The 100 KHz analog channel network 14 comprises an oscillator 76 connected through a series switch 78 to a power amplifier 80. The connecting leads A, B and C to the transmitter logic network 29 are shown. Lead A is connected to the output of the 100 KHz oscillator 76, load B is connected to an input of the 100 KHz series switch 78 and lead C connects to an input of the 27.12 series switch 72. Each of the power amplifiers 74, 80 is preferably connected to its respective resonant circuit 28, 28 via a coaxial cable as discussed hereinabove. In each channel, the series switch gates the signal from the appropriate oscillator to the amplifier as a function of the controlling logic. The 100 KHz oscillator 76 is also used to develop all of the timing functions required by the digital portion of the receiver 30 to be described hereinafter.

Connected to the 100 KHz series switch 78 is an output of a program logic circuit 84 in the transmitter logic network 29 to which is coupled a full decoder network 88. A time duration counter circuit 86 is connected to the counter full decoder network 88. Another output of the program logic circuit 84 is connected to a data register 90, a data decoder 92 and a mode logic circuit 94. The output of the data register 90 is connected to the data decoder 92 which is coupled to a summing network or junction 96 as is a 5-microsecond stimulation trigger output of the mode logic circuit 94. The mode logic circuit 94 is additionally coupled to a multiplexer 98 and to a stimulating counter 112 to which it provides a presetting signal. The output of the stimulating counter 112 is connected to a counter full decoder circuit 114 whose output is fed back to the mode logic circuit 94. A digital frequency divider 116 is connected to the output of the 100 KHz oscillator to feed clock signals of 0.1 Hz and 10 KHz, for example, as required to selected circuits such as the time duration counter 86 and to the stimulating counter 112, respectively. A power supply 118, operating from a 60 Hz power source, provides all of the operating voltages for the transmitter.

Prior to activating the transmitter, the operating instructions listed in FIGS. 1 and 4 are entered into the transmitter via suitable switches such as the rotary thumbwheel and selector switches shown in FIG. 3. The transmitter converts this information into a digital sequence of words that are transmitted to the implanted receiver 30 at the appropriate time. The transmitter 10 is activated by the A-C Power Switch which supplies the +5 volts and ±15 volts to the appropriate electronics via the power supply 118. No signals are transmitted from the transmitter at this time. When the Stimulate Switch is activated, the 100 KHz series switch 78 is immediately closed which causes the 100 KHz power signal to be inductively coupled to the resonant circuit 36 in the receiver. No 27.12 MHz signal is transmitted yet because the preset memory pulse of the receiver has just been activated by the power supply 38 and it must be allowed to decay to insure proper reception. Approximately one millisecond after activation of the Stimulate Switch, the program logic circuit 84 enables the data register 90 and the data decoder 92 which operate together to read the Data Completion Pulse (1 bit), the Positive Amplitude (10 bits) and the Negative Amplitude (10 bits) that have been previously entered into the transmitter; connect these data into binary bits where a low state or "0" is 5 microseconds in width and a high state or "1" in 50 microseconds in width; and encode this information onto a 27.12 MHz r-f signal by turning on the 27.12 MHz series switch 72 as required. This 21-bit pulse width modulated Amplitude Data Word is then serially transmitted to the receiver 30 only once.

The program logic circuit 84 permanently inhibits the data register 90 and the data decoder 92 after the 21-bit Amplitude Data Word has been transmitted and it also enables the mode logic circuit 94. The mode logic circuit 94 momentarily presets the stimulating counter 112 via the multiplexer 98 to a count value specified by the Positive Pulse Duration. The 10 KHz clock signal from the digital frequency divider 116 now causes the stimulating counter 112 to increase its count until it is full. This state is sensed by the counter full decoder 114 which causes the mode logic circuit 94 to momentarily preset the stimulating counter 112 via the multiplexer 98 to a count value specified by the Negative Pulse Duration. The foregoing sequence is automatically repeated, with the Interpulse Duration, the Positive Pulse Duration and the Negative Pulse Duration, etc., being used to preset the stimulating counter 112. Each time the stimulating counter 112 is reset by the mode logic circuit 94, a 5-microsecond pulse is generated by the mode logic circuit 94 which gates the 27.12 MHz series switch 72 through the summing junction 96 to generate another bit of the 3-bit Stimulating Word.

The Pulse Mode Selector Switch allows the user to determine which one of the five stimulating signals shown in FIGS. *5b, c, d, f* and *h* should be used to stimulate the nerve. From the basic Stimulation Word, the user can select either a bipolar pulse, unipolar positive pulse, or unipolar negative pulse stimulation via the Pulse Mode Selector Switch, depending upon the negative and positive amplitudes that have been entered into the transmitter via the data register 90. The "+DC" mode modifies the operation of the mode logic circuit 94 by inhibiting its recycling operation after the initial presetting of the stimulating counter 112; thus only the "ON+"b bit of the stimulation word is transmitted as shown in FIG. *5e*. The "−DC" mode modifies the mode logic circuit 94 in a similar manner except that only the "ON+"b pulse (at zero microamperes positive amplitude) and the "ON−" pulse are transmitted before the mode logic circuit 94 recycling operation is inhibited.

The Time Mode Selector Switch for the Program Logic Circuit 84 determines the time duration that the nerve will be stimulated. The Single Cycle mode selection will allow the transmitter to transmit only one Stimulation Word. Selection of the Program mode will allow stimulation to occur only for the Program Time Duration which has previously been entered into the transmitter through the time duration counter 86. The method of operation is functionally identical to that of the stimulating counter 112 and its associated counter full decoder 114, with the 0.1 Hz clock signal used in lieu of the 10 KHz clock signal. The Continuous mode selection via the Time Mode Selector Switch will allow stimulation to continue uninterrupted until the Stimulate Switch is deactivated.

Stimulation of the nerve will cease whenever the Stimulate Switch is deactivated and the Stimulation Word is completed. This function is performed automatically when the Time Mode Selector Switch is in either the Single Cycle mode or the Continuous mode. Deactivation of the Stimulate Switch will shut off the 100 KHz power signal as soon as the Stimulation Word has been completed.

Several different types of transmitters may be used with the implantable receiver 30. Selection will depend upon the particular need. The laboratory transmitter shown in FIG. 4 and described hereinabove would be used by professional personnel in hospitals, clinics and doctors' offices to collect experimental and diagnostic data and to determine the fixed program parameters to be prescribed for the patient's personal pre-programmed transmitter. The pre-programmed transmitter is available in at least two other configurations: the bedside transmitter and the portable transmitter. Both versions are functionally identical to the laboratory transmitter except that the operating instructions such as stimulating levels, polarities, time durations, etc., discussed hereinabove, will be pre-programmed. The bedside transmitter will ordinarily use conventional 115V a-c power for its operation whereas the portable unit will be battery operated.

The receiver 30 provides a basic bipolar constant current waveform to the nerve from which four other stimulating modes can be externally selected. Utilizing the circuitry described herein, the time duration of any polarity pulse can be varied in real-time from 20 microseconds to 10 seconds in 10 microsecond intervals. The positive and negative amplitudes of these current pulses can be externally selected from 0 microamperes to 4 milliamperes in 10 microamperes intervals. A pulse repetition of 0.03 Hz to 16.7 KHz can be obtained, for example. The shape of the current pulses will generally always be rectangular, having a 0 to 90 percent rise and fall time of less than 3 microseconds.

As previously expressed hereinabove, five types of stimulating signals may be applied to a nerve, for example. Referring again to FIGS. *5a–5h*, the basic bipolar waveform available from the receiver 30 is shown at *5b*. This corresponds to the basic stimulation word shown at *5a*. By setting either the negative or positive polarity to 0 microampere, a positive unipolar current pulse *5c* or a negative unipolar current pulse *5d* can be obtained. A programmable steadystate current level of either polarity can also be generated from either unipolar current pulse by extending the time duration of the current pulse as shown at *5f* and *5h*. The stimulation currents shown at *5f* and *5h* correspond to the DC stimulation words shown at *5e* and *5g*, respectively.

The receiver 30 can be divided into two major sections: the power supply circuit 38 and the signal processor network 50. The function of the power supply circuit 38 is to generate the required electrical power for the implanted electronics and to provide two control signals to the signal processor network 50. The 100 KHz tuned center-tapped coil 32 is used as the secondary of the power double-tuned coupling circuit 20, 36 to develop the 100 KHz power signal. This signal is rectified, filtered, and regulated to provide stable operating voltages for the electronics. The Memory Preset and Safety Release control signals are generated from the supply voltages to preset the memory circuit and release the safety shunt circuit, respectively. These latter circuits will be more fully explained hereinafter.

The function of the signal processor network 50 is to receive, demodulate, and process all operational instructions that are sent from the transmitter 10 and to generate with the aid of the power supply the proper stimulating amplitude, polarity and time duration signal. The 27.12 MHz tuned coil 44 is used as a secondary of the signal doubletuned coupling circuit 28, 48 to develop the instructions that were sent from the transmitter. The first 21 bits of instructions is the Amplitude Data Word which is demodulated and stored in the receiver memory circuit. All remaining bits are considered as stimulation instructions and are demodulated and decoded as such. These stimulation instructions select either the Negative Amplitude Word or the Positive Amplitude Word or neither word from the receiver memory circuit. The selected amplitude word, if selected, is converted to an analog signal which controls the inverting constant current amplifier. This amplifier then forces the proper constant current signal through the nerve and will be more fully discussed hereinafter.

Referring now to FIG. 6, the receiver 30 is shown as comprising the power supply circuit 38 which includes the 100 KHz tuned circuit 36 connected to a full-wave rectifier 120 which provides positive and negative unregulated voltages to respective voltage regulators 122, 124. The negative unregulated voltage from the full-wave rectifier 120 is also connected to a safety shunt control circuit 126. In addition to supplying the posi-

tive operating voltage to the signal processor network 50, the output of the positive voltage regulator 122 is connected to a preset circuit 128. The output of the negative voltage regulator 124 supplies the negative operating voltage to the signal processor network 50.

In the signal processor network 50 the 27.12 MHz tuned circuit 48 is connected to an r-f demodulator 130 whose output is interconnected with a 21-bit shift register (memory) 132 to couple in the overall Data Signal, and to a mode logic circuit 134 and a stimulation decoder 136 to provide the necessary clock pulses. The mode logic circuit 134 has one output connected to provide a Shift Register Clock to the 21-bit shift register 132 and another output connected to provide a Stimulation Inhibit Signal to the stimulation decoder 136. Also coupled to the shift register 132 is a Memory Preset Signal from the output of the preset circuit 128 in the power supply 38. The shift register 132 has an output connected to provide a Data Completion Pulse to the mode logic circuit 134. A 10-line output (for the 10 bits) is connected to provide the Positive Amplitude Word to a positive word multiplexer 138, and another 10-line output (for the other 10 bits) is connected to provide the Negative Amplitude Word to a negative word multiplexer 140. An output of the stimulation decoder 136 is connected to the negative word multiplexer 140 and provides the "ON−" Signal. A second similar output from the stimulation decoder 136 provides the "ON+" Signal to the multiplexer 138. A third output from the stimulation decoder 136 provides an "OFF" Signal and it is coupled to an interpulse shunt circuit 142 the output of which is connected to receiver output conductors 52, 54. A 10-line output of the positive word multiplexer 138 is connected to a positive digital-to-analog converter 144 whose output in turn is coupled to an inverting X4 current amplifier 146. A 10-line output of the negative word multiplexer 140 is connected to a negative digital-to-analog converter 148. The outputs of both converters 146, 148 are coupled to an inverting constant current amplifier 150 whose output is connected to receiver output conductors 52, 54. Also connected to receiver output conductors 52, 54 is a safety shunt circuit 152 which receives a safety release signal as appropriate from the safety shunt control circuit 126 in the power supply 38.

In operation, the digital instructions from the transmitter 10 are received by the 27.12 MHz tuned circuit 48 and fed to the r-f demodulator 130 which comprises a voltage doubler diode detector and a low pass filter. The pulsed r-f data signal from the transmitter 10 comprises the 21-bit Amplitude Data Word and a series of Stimulation Words. Each Stimulation Word comprises three 5-microseconds r-f pulses. The r-f demodulator 130 converts the pulsed 27.12 MHz r-f signal to a rectified positive video signal which serves as the Clock. The Clock Signal is used in three separate applications: it passes through the low pass filter which serves as a pulse width discriminator to derive the Data Signal for the 21-bit shift register 132, it is used in the mode logic circuit 134 to generate the Shift Register Clock for the shift register 132, and it serves as a trigger signal to the stimulation decoder 136. Demodulation of the 3-bit Stimulation Word produces three Clock Signals and no Data Signals because each of the 3-bits is only 5 microseconds wide.

The 21-bit register 132, comprising a series grouping of 21 flip-flop circuits, functions as a memory. It stores a Data Completion Pulse, a Positive Amplitude Word and a Negative Amplitude Word. The memory is initially cleared by the Memory Preset Signal which is generated by the preset circuit 128 in the power supply 38. the 21-bit Amplitude Data Word is transmitted only after the Memory Preset Signal has been utilized. The Amplitude Data Word enters into the shift register 132 on the positive slope of the Shift Register Clock. The Shift Register Clock is an inverted version of the Clock signal which is gated depending upon whether the receiver system is in the "receive data" mode or "stimulation" mode. The 1-bit Data Completion Pulse enters into the shift register 132 first. It is followed by a 10-bit word which represents the negative stimulating current amplitude and another 10-bit word which represents the positive stimulating current amplitude word. These 21 bits of information are called the Amplitude Data Word, as mentioned previously hereinabove. When the Data Completion Pulse has been shifted into the end position of the shift register 132, the Shift Register Clock is inhibited by the mode logic circuit 134 which converts the shift register into a static memory.

The mode logic circuit 134 which comprises two NOR gates determines if an inverted version of the Clock is to go to the shift register 132 as the Shift Register Clock or if it can be processed by the stimulation decoder 136. The absence of the Data Completion Pulse indicates that the memory is not full. This forces the Stimulation Inhibit Signal to be active which inhibits the stimulation decoder 136 while generating and applying the Shift Register Clock to the memory. The presence of the Data Completion Pulse indicates that the memory is full which causes the Shift Register Clock and the Stimulation Inhibit Signal to be deactivated. This essentially converts the shift register 132 to a static memory and allows the stimulation decoder 136 to be activated.

The stimulation decoder 136 is a "divide-by-three" counter with each state of the counter indicating the state of the Stimulation Word. These three states are used to generate the time duration and polarity of the stimulating output current to the nerve. The resulting three output signals ("ON+", "ON−", and "OFF") are mutually exclusive in that only one can be activated by any one time. The presence of the Stimulation Inhibit Signal disables the counter and forces the "OFF" to its activation state. The stimulation decoder 136 is activated only after the 21-bit shift register 132 is full. Only then is it permitted to count the number of Clock pulses to determine the state of the 3-bit Stimulation Word. The absence of the Stimulation Inhibit Signal then enables the stimulation decoder 136 which activates the "ON+" upon receiving the first clock pulse, the "ON−" upon receiving the second Clock pulse, and the "OFF" upon receiving the third Clock pulse. This process is then repeated as often as required. These outputs alternately select, via the positive word multiplexer 138 and the negative word multiplexer 140, the Positive Amplitude Word, the Negative Amplitude Word, or neither of the amplitude words. The latter condition occurs during the interpulse period and results in no stimulation of the nerve. Each of the mul-

tiplexers 138, 140 comprise a grouping of ten AND-OR gates. The polarity and amplitude of the nerve stimulation signal is achieved by digitally selecting either the stored Positive Amplitude Word or the stored Negative Amplitude Word. In each case the amplitude is represented by a 10-bit word. Two 10-bit multiplex switches, then, are used to select either of the two words or neither of them. In no case are both words selected simultaneously.

Conversion of the selected 10-bit digitally coded Amplitude Word and conversion of the "OFF Word" to an analog signal is performed by the digital-to-analog converters 144, 148. Each of the converters 144, 148 comprise a grouping of ten resistors each serially connected to the output of a selected AND-OR gate in its appropriate multiplexer circuit 138, 140. Each amplitude bit from the multiplexers is weighted by using a different value for each of the series resistors. The resulting currents which flow through the ten resistors in each converter 144, 148 are summed together to generate a current which is directly proportional to the digital code. No current results from a digital-to-analog converter which is fed from an "OFF" multiplexer. Summation of the positive amplitude is performed in the inverting X4 current amplifier 146 while the negative amplitude is summed in the inverting constant current amplifier 150, each of which comprise an operational amplifier circuit. In either case, the summing of the digital-to-analog decoding currents is performed by an operational amplifier which allows the summation to occur at zero volts. In this manner, the weighting current per decoding bit can be accurately established. The weighting currents for the Positive Amplitude Word are four times less than that of the Negative Amplitude Word so that less electrical power is consumed by the positive digital-to-analog converter 144.

The inverting X4 current amplifier 146 performs three functions: it sums together the weighting currents of the positive stimulation current; it inverts the polarity of the resulting current so that it will have a positive polarity at the output of the inverting constant current amplifier 150; and it amplifies the current level by a factor of four to be compatible with the Negative Amplitude Word.

The function of the inverting constant current amplifier 150 is threefold: it provides a constant current source with which the nerve will be stimulated; it sums together the weighting currents of the negative stimulation current; and it sums in the positive stimulating current from the inverting X4 current amplifier 146. The latter two functions are performed at zero volts to obtain the proper levels. These functions are performed in the inverting constant current amplifier 150 by a unity gain operational amplifier with the nerve being used as the feedback impedance.

The output current from the inverting constant current amplifier is effectively shunted out at various times by placing two low impedance shunt circuits in parallel across the nerve. The safety shunt circuit 152 comprises a field-effect transistor having a nominal 60 ohms impedance, for example, which is across the nerve at all times except when the power supply 38 is activated. The state of the safety shunt circuit 152 is controlled by the safety shunt control circuit 126 which comprises a low pass resistor-capacitor filter in which a diode is in parallel with a 1 megohm resistor to generate the Safety Release Signal. This signal is a modified version of the unregulated negative supply voltage from the full wave rectifier 120 and differs from it only in that an unsymmetrical time delay has been introduced. The time delay occurs only when the negative voltage is being increased. The absence of the negative supply, which may be due to the lack of the 100 KHz continuous wave power signal or due to a circuit malfunction, will result in having the 60-ohm safety shunt circuit 152 across the nerve. Only when the negative supply is present will the low impedance shunt of the safety shunt circuit 152 be removed. The other shunt is the interpulse shunt circuit 142 comprising another field-effect transistor having a nominal 75 ohms impedance, for example, which is also across the nerve at all times except when the "ON+" and "ON−" states of the Stimulation Word are activated. At these times, the interpulse shunt circuit 142 receives the "OFF" Signal from the stimulation decoder 136. When the system is not activated, the two separate shunt circuits are across the nerve to insure that no extraneous signal pick-up by the system will introduce unwanted currents to the nerve. Failure to have both power supply voltages present will automatically place one of the shunts across the nerve. This provides a most desirable safety feature.

The 100 KHz continuous wave power signal received by the 100 KHz tuned circuit 36 is converted into positive and negative d-c voltages. These voltages are filtered and regulated in their respective voltage regulators 122 and 124 to provide stable supply voltages for the receiver circuits. The function of the preset circuit 128 is to generate the Memory Preset Signal which is a short duration positive pulse that presets the shift register 132 to zero. The Memory Preset Signal is generated from the regulated positive supply of the positive voltage regulator 122 when the power supply 38 is first activated. The preset circuit 128, in its simplest form, comprises a high pass filter that differentiates the regulated positive voltage received from the positive regulator 122. In another slightly more complex form, the preset circuit 128 may be a voltage-sensing circuit comprising a serially connected input field-effect transistor, zener diode and resistor-to-ground combination connected in parallel across a serially connected resistor and grounded-emitter NPN transistor combination. A capacitor is connected across the zener diode-resistor series subcombination from the negative terminal of the zener diode to the ground side of the resistor. The base of the NPN transistor is connected to the positive terminal of the zener diode; and the collector, connected to the field-effect transistor through the series resistor in the NPN circuit, provides the Memory Preset Signal output. The field-effect transistor acts like a constant current diode in this circuit. Besides presetting the memory of the shift register 132 to zero, this alternative preset circuit clears the memory and returns the operation back to the "enter data mode" from the stimulation mode, if the positive voltage supply drops below a preset value. Such a situation can arise, for example, by moving the transmitter probe too far away from the implanted receiver during operation of the system.

A summary of the operation of the system is as follows:

TIMING SEQUENCE

Operation of the system requires four operational time modes. First the 100 KHz power is turned on so that the power supply 38 can generate the required voltages for the implanted electronics. Second, the desired pulse amplitudes are transmitted via the Amplitude Data Word to the signal processor 50 in digital form where they are decoded and stored. This phase requires approximately 4,200 microseconds. Third, stimulation of the nerve may now begin in real-time. This phase of the operation will last as long as nerve stimulation is required. Fourth, stimulation is terminated by inhibiting the stimulating word immediately after the "OFF" bit is transmitted and then turning off the 100 KHz power.

The sequence of events which occurs in each of the four time modes is listed below:

Mode 1, Turn-On

a. 100 KHz transmitter signal is activated.
b. Implantable power supply 38 is activated.
c. Memory cells are preset to "0" via the Memory Preset Signal from the power supply 38.
d. Safety Shunt 152 is activated to remove its 60 ohm shunt impedance from across the output 52, 54.
e. Signal processor 50 is in "enter data" status with the stimulation decoder 136 inhibited.

Mode 2, Transmit Data:

a. 21-bit Amplitude Data Word is serially transmitted.
b. Amplitude word is decoded and stored.
c. Memory 132 is inhibited as the stimulation decoder 136 is activated.
d. Signal processor 50 is in "stimulation" mode.

Mode 3, Stimulate

a. The first bit of the three-bit Stimulating Word will remove the interpulse shunt 142 and will cause the programmed positive current to flow through the nerve.
b. The second bit of the Stimulating Word will shutoff the positive current and will cause the programmed negative current to flow through the nerve.
c. The third pulse of the Stimulating Word will shutoff the negative current and activate the interpulse shunt 142 across the nerve.
d. Further stimulation of the nerve can be obtained by repeating the above steps (a through c).

Mode 4, Turn-Off

a. The Stimulation Word is inhibited immediately after the "OFF" bit is transmitted. (The interpulse shunt 142 is deactivated to place a low impedance across the output 52 and 54).
b. The 100 KHz power signal is shut-off.
c. The safety shunt 152 is deactivated to place a low impedance across the output 52 and 54.

TRANSMISSION AND STORAGE OF THE AMPLITUDE DATA WORD:

The desired stimulating amplitudes are transmitted as a coded 20-bit binary word along with the 1-bit Data Complation Pulse. Because of the ease of implementing the transmitted logic network 29, a binary coded decimal format (BCD) is used instead of a coded binary format.

The signal processor 50 receives this word, demodulates it and stores the coded amplitude bits in its memory. When the Data Completion Pulse has gone through all of the flip-flops in the shift register 132 and is finally entered in the last flip-flop, the shift register 132 is locked by inhibiting its clock and now is employed as a static memory.

During this data transmission mode no stimulation of the nerve is performed. In fact, the interpulse shunt 142 is deactivated and places a nominal 75 ohm impedance across the nerve to prevent voltage buildup on the nerve and to shunt any demodulated signals that might stimulate the nerve.

The presence of the Data Completion Pulse in the last flip-flop signifies that the Amplitude Data Word has been entered into the shift register 132 and that stimulation of the nerve can now be performed in real-time as commanded by the transmitter 10.

TRANSMISSION AND UTILIZATION OF THE STIMULATION WORD(S):

Stimulating instructions from the transmitter will normally be encoded into a repetitive 3-bit pulse positioned modulated Stimulation Word(s). Each Stimulation Word consists of three 5-microsecond r-f pulses which are decoded to derive the time period of each portion of the basic bipolar waveform. The time duration of the Negative Pulse Duration, Positive Pulse Duration, and Interpulse Duration is determined by the transmitter from the data entered into it via the thumbwheel switches. The two abbreviated Stimulation Words as described hereinabove are utilized for the + and − DC Modes.

The stimulation decoder 136 provides three outputs which control the state of the current pulse to the nerve. These three controls are mutually exclusive in that only one can be on at any one time. The "ON+" signal enables only the positive digital-to-analog converter 144 which causes the specified positive stimulating current to flow through the nerve. The "ON−" signal enables only the negative digital-to-analog converter 148 which causes the specified negative stimulating current to flow through the nerve. The "OFF" signal deactivates the interpulse shunt which places the nominal 75 ohm shunt impedance across the nerve to avoid voltage build-up and to reduce the dc leakage level.

I claim:

1. An electronic system for the stimulation of a biological system in a living body, said system comprising:

a. transmitter means adapted to be operably associated externally of said living body for generating transmitted pulses of radio frequency energy at a first frequency and for additionally generating transmitted signals of continuous wave energy at a second frequency, said pulses of radio frequency energy including digital stimulation signals for stimulating said biological system, said continuous wave energy including power signals for providing operating voltages in said system;

b. said transmitter means including transmitter logic network means for receiving and processing stimulation and power signal information;

c. said transmitter means additionally including first and second analog channel network means operably connected to said transmitter logic network means and responsive thereto, said first analog channel network means generating said pulses of radio frequency energy at said first frequency containing said digital stimulation signals, said second analog channel network means generating said continuous wave energy at said second frequency containing said power signals;

d. said transmitter means further including first and second resonant circuit means operably connected to said first and second analog channel network means, respectively, and responsive thereto, said first resonant circuit means resonant at substantially said first frequency for transmitting said pulses of radio frequency energy containing said digital stimulation signals, and said second resonant means resonant at substantially said second frequency for transmitting said continuous wave energy containing said power signals;

e. receiver means adapted to be operably positioned within said living body for receiving said pulses of radio frequency energy containing said digital stimulation signals at said first frequency and for additionally receiving said continuous wave energy containing said power signals at said second frequency as transmitted from said transmitter means;

f. said receiver means including third and fourth resonant circuit means responsive to said second and first resonant circuit means, respectively, said third resonant circuit means resonant at substantially said second frequency for receiving said transmitted continuous wave energy containing said power signals, and said fourth resonant circuit means resonant at substantially said first frequency for receiving said transmitted pulses of radio frequency energy containing said digital stimulation signals;

g. said receiver means additionally including power supply circuit means operably connected to said third resonant circuit means and responsive to said continuous wave energy containing said power signals received by said third resonant circuit means for providing said operating voltages for said receiver means; and

h. said receiver means further including signal processor network means operably connected to said power supply circuit means and to said fourth resonant circuit means, said signal processor network means responsive to said operating voltages from said power supply circuit means and additionally responsive to said pulses of radio frequency energy containing said digital stimulation signals at said first frequency for providing stimulating signals to said biological system.

2. The electronic system defined in claim 1, wherein said first, second, third and fourth resonant circuit means each comprise in combination a capacitor and an associated inductor, said inductors of said first and fourth resonant circuit means each being an antenna operable substantially at said first frequency and said inductors of said second and third resonant circuit means each being an antenna operable substantially at said second frequency.

3. The electronic system defined in claim 1, wherein said first analog channel network means comprises oscillator means for generating said radio frequency energy at said first frequency, switch means coupled to said oscillator means responsive to said transmitter logic network means for combining said radio frequency energy at said first frequency with said digital stimulation signals, and amplifier means connected to said switch means for amplifying signals received through said switch means.

4. The electronic system defined in claim 1, wherein said second analog channel network means comprises oscillator means for generating said continuous wave energy at said second frequency, switch means coupled to said oscillator means responsive to said transmitter logic network means for combining said continuous wave energy at said second frequency with said power signals, and amplifier means connected to said switch means for amplifying signals received through said switch means.

5. The electronic system defined in claim 1, wherein said signal processor network means includes:

a. a radio frequency demodulator operably connected to said fourth resonant circuit means and responsive thereto;

b. shift register means operably connected to said radio frequency demodulator for receiving a data signal from said radio frequency demodulator and for providing a positive amplitude word, a negative amplitude word and a data completion pulse, said shift register means also operably connected to said power supply circuit means for receiving a memory reset signal therefrom.

c. mode logic circuit means operably connected to said radio frequency demodulator and to said shift register means for receiving a clock signal from said radio frequency demodulator and for receiving said data completion pulse from said shift register means, said mode logic circuit means providing a shift register clock also said shift register means and for providing a stimulation inhibit signal;

d. stimulation decoder means operably connected to said radio frequency demodulator and to said mode logic circuit means for receiving a triggering clock signal from said radio frequency demodulator and for receiving said stimulation inhibit signal from said mode logic circuit means, said stimulation decoder means s providing mutually exclusive output signals including "ON+", "ON−" and "OFF" signals;

e. positive word multiplexer means operably connected to said shift register means and to said stimulation decoder means for receiving and selecting said positive amplitude word from said shift register means and for receiving said "ON+" signal from said stimulation decoder means;

f. negative word multiplexer means operably connected to said shift register means and to said stimulation decoder means for receiving and selecting said negative amplitude word from said

shift register means and for receiving said "ON" signal from said stimulation decoder means;

g. negative digital-to-analog converter means operably connected to said negative word multiplexer means and responsive thereto for converting said negative amplitude word to an analog signal;

h. positive digital-to-analog converter means operably connected to said positive word multiplexer means and responsive thereto for converting said positive amplitude word to an analog signal;

i. inverting X4 current amplifier means operably connected to said positive digital-to-analog converter means and responsive thereto for providing an output signal amplified by substantially a factor of four to be compatible with said negative amplitude word;

j. inverting constant current amplifier means operably connected to said inverting X4 current amplifier means and to said negative digital-to-analog converter means and responsive thereto for providing said stimulating signals to said biological system; and

k. shunt circuit means operably connected to said stimulation decoder means and to said power supply circuit means for receiving said "OFF" signal from said stimulation decoder means and for receiving a safety release signal from said power supply circuit means to provide protection against undesired stimulating signals.

6. The electronic system defined in claim 5, wherein said shunt circuit means comprises interpulse shunt circuit means operably connected to said stimulation decoder means for receiving said "OFF" signal and safety shunt circuit means operably connected to said power supply circuit means for receiving said safety release signal, said interpulse shunt circuit means and said safety shunt circuit means operably coupled in parallel across said biological system.

7. The electronic system defined in claim 1, wherein said power supply circuit means comprises:

a. full-wave rectifier means operably connected to said third resonant circuit means and responsive thereto for converting said continuous wave energy received from said third resonant circuit means into positive and negative d-c voltages;

b. positive voltage regulator means operably connected to said full-wave rectifier means for receiving said positive d-c voltages from said full-wave rectifier means and for providing regulated positive operating voltages for said receiver means;

c. preset circuit means operably connected to said positive voltage regulator means and responsive thereto for providing a memory preset signal comprising a short duration positive pulse for said receiver means;

d. negative voltage regulator means operably connected to said full-wave rectifier means for receiving said negative d-c voltages from said full-wave rectifier means and for providing regulated negative operating voltages for said receiver means; and

e. safety shunt control circuit means operably connected to said negative voltage regulator means and responsive thereto for providing a safety release signal for said receiver means.

8. A transmitter for generating transmitted pulses of radio frequency energy at a first frequency containing digital stimulation signals for the stimulation of a biological system in a living body and for additionally generating transmitted signals of continuous wave energy at a second frequency containing power signals, said transmitter comprising:

a. logic network for receiving and processing stimulation and power signal information;

b. first and second analog channel network means operably connected to said logic network means and responsive thereto, said first analog channel network means generating said pulses of radio frequency energy at said first frequency containing said digital stimulation signals, said second analog channel network means generating said continuous wave energy at said second frequency containing said power signals, said first analog channel network means including:

1. first oscillator means for generating said radio frequency energy at said first frequency,

2. first switch means coupled to said first oscillator means responsive to said logic network means for combining said radio frequency energy at said first frequency with said digital stimulation signals, and

3. first amplifier means connected to said first switch means for amplifying signals received through said first switch means,

said second analog channel network means including:

1. second oscillator means for generating said continuous wave energy at said second frequency,

2. second switch means coupled to said second oscillator means responsive to said logic network means for combining said continuous wave energy at said second frequency with said power signals, and

3. second amplifier means connected to said second switch means for amplifying signals received through said second switch means; and

c. first and second resonant circuit means operably connected to said first and second analog channel network means, respectively, and responsive thereto, said first resonant means resonant at substantially said first frequency for transmitting said pulses of radio frequency energy containing said digital stimulation signals, and said second resonant circuit means resonant at substantially said second frequency for transmitting said continuous wave energy containing said power signals.

9. The transmitter defined in claim 8, wherein said first and second resonant circuit means each comprise in combination a capacitor and an associated inductor, said inductor of said first resonant circuit means being an antenna operable substantially at said first frequency and said inductor of said second resonant circuit means being an antenna operable substantially at said second frequency.

* * * * *

United States Patent [19]

Wingrove

[11] **3,833,005**

[45] **Sept. 3, 1974**

[54] COMPARED COUNT DIGITALLY CONTROLLED PACEMAKER

[75] Inventor: **Robert C. Wingrove, Circle Pines, Minn.**

[73] Assignee: **Medtronic, Inc., Minneapolis, Minn.**

[22] Filed: **July 26, 1971**

[21] Appl. No.: **166,219**

[52] U.S. Cl. ..... **128/419 P, 128/422**

[51] Int. Cl. **A61n 1/36**

[58] Field of Search ..... 128/419 C, 419 E, 419 P, 128/419 R, 421, 422; 307/220, 231; 340/146.2

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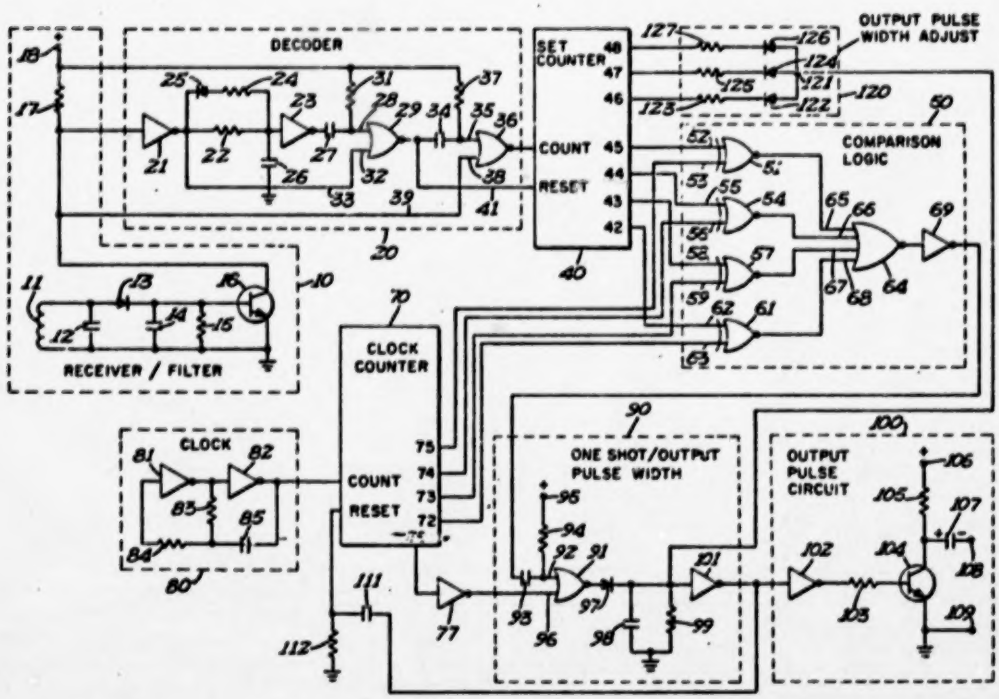
[57] **ABSTRACT**

A cardiac pacer having adjustable rate and/or pulse width controls controlled by digital means including a first counter for receiving information and storing the data, a second counter connected to clock means, and logic means for comparing the outputs of the first and second counters to determine pulse rate and width. The preferred embodiments of the digitally controlled pacer include means connected to the first counter for receiving coded set signals and rejecting noise and other interference signals. The preferred embodiment of a transmitter for sending coded signals to the pacer is also shown, the transmitter being digitally operable to provide coded bursts of RF pulses to the pacer receiver.

25 Claims, 4 Drawing Figures



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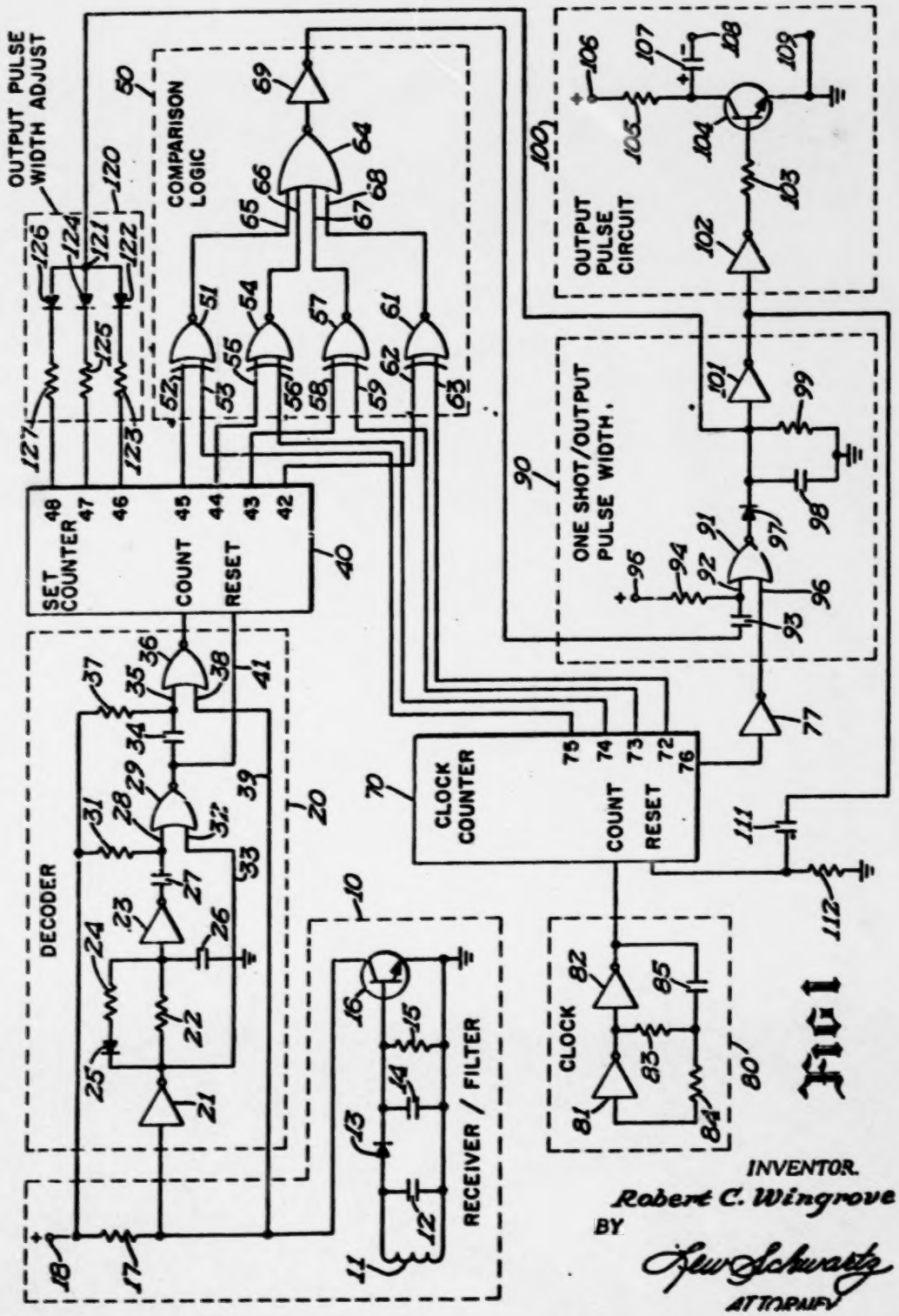

FIG 1

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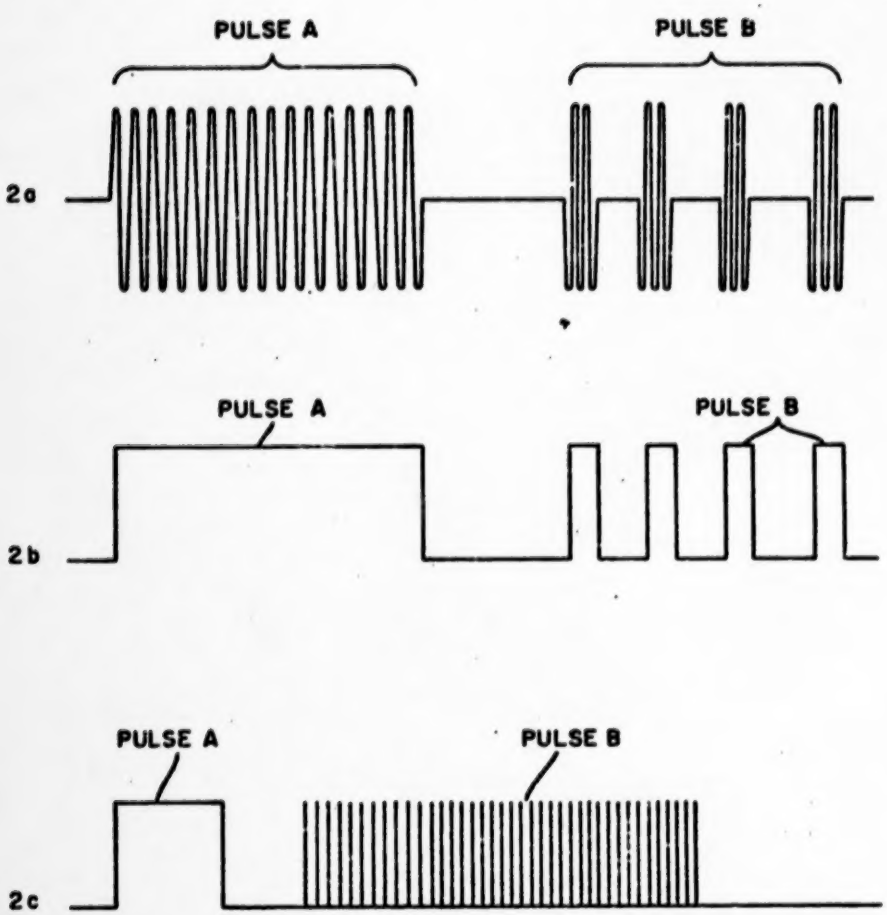

Fig 2

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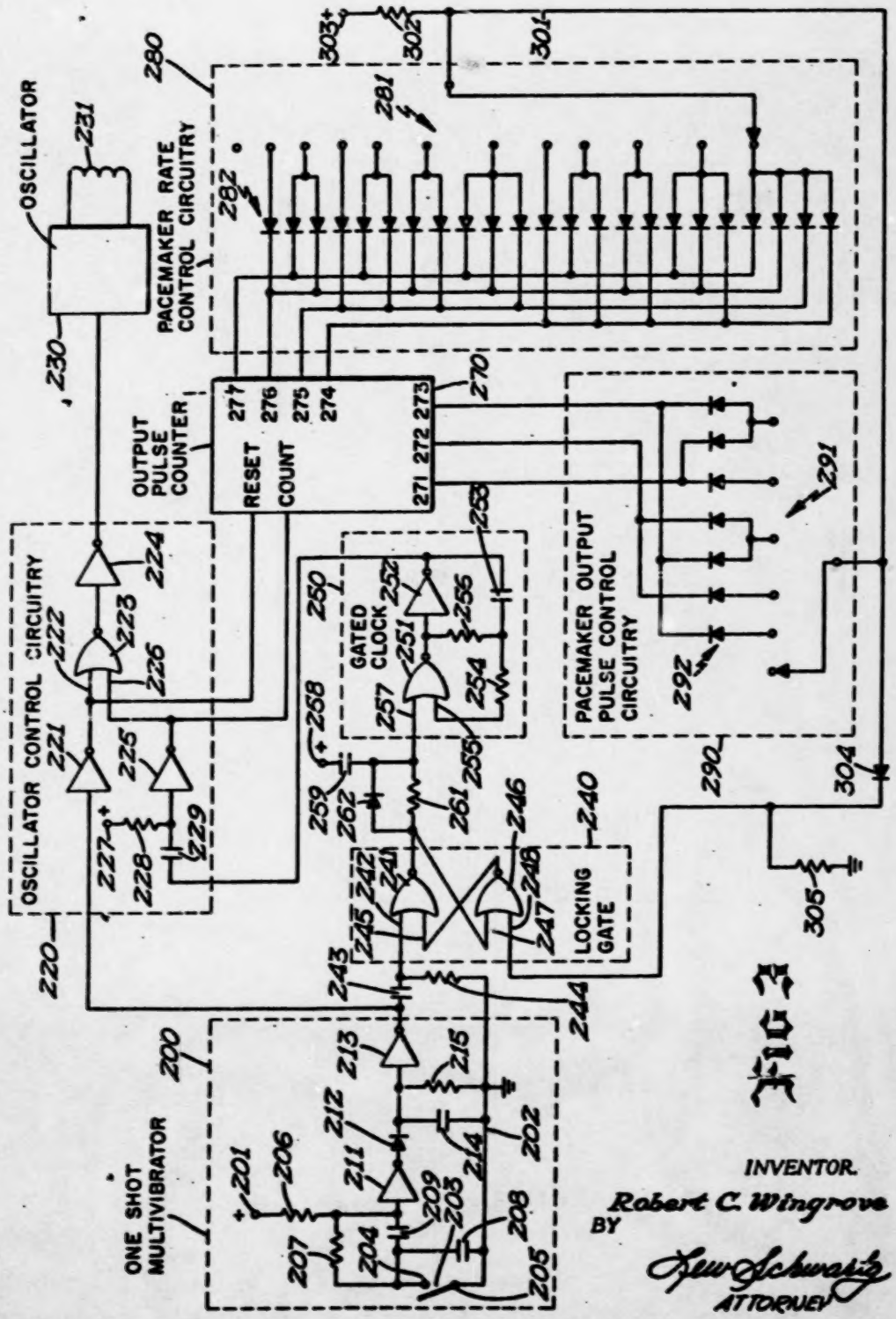

FIG 3

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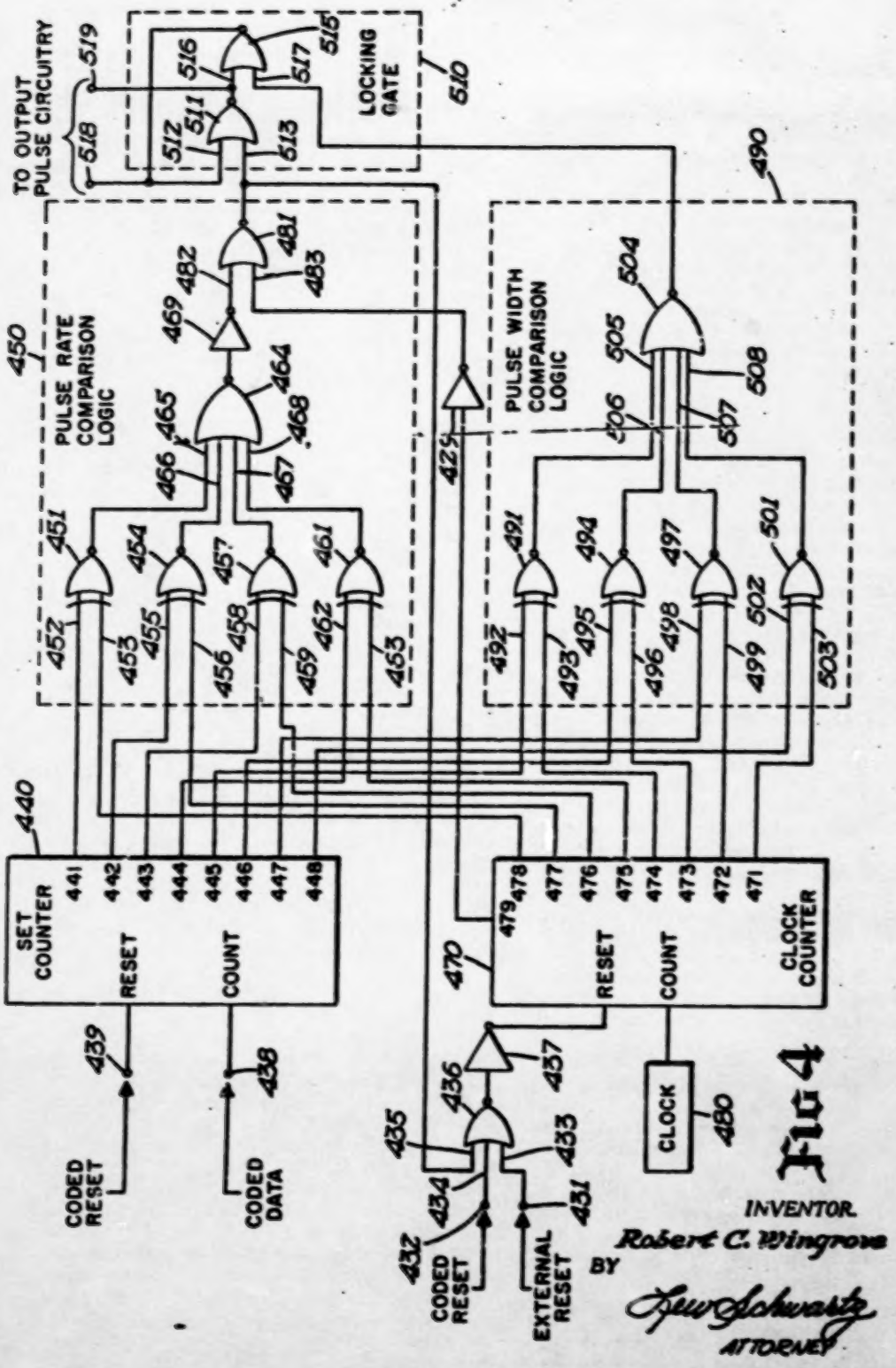

Fig 4

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COMPARED COUNT DIGITALLY CONTROLLED PACEMAKER

BACKGROUND OF THE INVENTION

Cardiac pacers and other implantable stimulation devices are well known by those reasonably skilled in the art. A search is continually under way to produce an improved device which has a simple programing capability for rate and amplitude control, for example, which has an input error protection to prevent noise signals from causing dangerous situations, which is safe, and which has as low as possible power consumption. The apparatus of this invention provides these and other advantages over the prior art by utilizing a digital approach to what has for the most part been done in analog circuitry in the prior art, and by providing circuits which can be reduced to integrated circuitry to thus provide a minimum power drain. Such advantages of a digital approach are known in the prior art, as for example U.S. Pat. No. 3,557,796.

SUMMARY OF THE INVENTION

Briefly described, the pacer apparatus of this invention includes a memory in the form of a first digital counter, and a second digital counter connected to continually count a digital clock. A first network of a logic circuitry interconnects the first and second counters for purposes of comparing outputs. When the output of the second digital counter is the same as that of a portion of the memory to which it is being compared, an output signal is provided from the logic circuitry. This output signal triggers a pacemaker output pulse which travels to electrodes adapted to be connected to the heart. The data for the memory is provided, in the preferred embodiment, through an RF receiver-filter which is connected to the memory through a decoder network. The decoder network or circuitry is provided to prevent the passage of extraneous 60 cycle noise signals and to prevent the passage of almost all conceivable noise signals. The pacer apparatus of this invention also includes further circuit means connected to the first counter and to the pacer output pulse circuitry for determining pulse width according to the information stored in the memory.

The coded RF input pulses are provided, in the preferred embodiment, by a transmitter which includes yet another digital counter, the outputs of which are selectable to provide the desired data to the memory in the pacer apparatus. The selected data is transmitted in coded form automatically by the transmitter.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of the digital pacemaker apparatus of this invention;

FIGS. 2*a*, *b*, and *c* comprise graphs of the coded pulse input to the apparatus of FIG. 1 for providing data to the memory;

FIG. 3 is a schematic diagram of the transmitter apparatus of this invention which provides data to the apparatus of FIG. 1; and

FIG. 4 is another embodiment of the pacer apparatus of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1 there is shown a receiver-

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filter 10 comprising a coil 11 across which is connected a capacitor 12. A diode 13 and a capacitor 14 are connected in series across capicitor 12. A resistor 15 is connected across capacitor 14. A transistor 16 has its base connected to one side of resistor 15 and its emitter connected to the other side of resistor 15. The emitter of transistor 16 is also connected to ground, while the collector of transistor 16 is connected through a resistor 17 to a positive power input terminal 18.

There is also shown a decoder 20 which is used to greatly decrease the likelihood of extraneous noise signals affecting the pacer. Decoder 20 includes an inverter 21 which has an input connected to the collector of transistor 16. The output of inverter 21 is connected through a resistor 22 to the input of another inverter 23. A resistor 24 and a diode 25 are connected in series across resistor 22. The input of inverter 23 is also connected through a capacitor 26 to ground. The output of inverter 23 is connected through a capacitor 27 to an input 28 of a two-input positive nor logic gate 29. Input 28 of gate 29 is also connected through a resistor 31 to power input terminal 18. The other input 32 of gate 29 is connected by a lead 33 to the output of inverter 21. The output of gate 29 is connected to a capacitor 34 to an input 35 of another two-input positive nor logic gate 36. Input 35 is also connected to a resistor 37 to power input terminal 18. The other input 38 of gate 36 is connected by a lead 39 to the collector of transistor 16.

In FIG. 1 there is also shown a set counter 40 for receiving the decoded external signal. The output of gate 36 is connected to the count input terminal of counter 40, which is connected as a digital counter having a plurality of outputs including outputs 42, 43, 44, 45, 46, 47, and 48. A reset terminal of counter 40 is connected through a line 41 to the output of gate 29.

There is also shown a comparison logic circuit 50, comprising four two-input exclusive or gates 51, 54, 57 and 61 as well as four-input positive nor logic gate 64 and an inverter 69. An input 52 of gate 51 is connected to counter output terminal 45. An input 55 of gate 54 is connected to counter output terminal 44. An input 58 of gate 57 is connected to counter output terminal 43. An input 62 of gate 61 is connected to counter output terminal 42. The output of gate 51 is connected to an input 65 of gate 64. The output of 54 is connected to an input 66 of gate 64. The output of gate 57 is connected to an input 67 of gate 64. The output of gate 61 is connected to an input 68 of gate 64. The output of gate 64 is connected to the input of inverter 69.

There is also shown a clock counter 70 which has a plurality of count output terminals including terminals 72, 73, 74, 75 and 76. Terminal 72 is connected to an input 63 of gate 61. Terminal 73 is connected to an input 59 of gate 57. Terminal 74 is connected to an input 56 of gate 54. Terminal 75 is connected to an input 53 of gate 51.

There is also shown in FIG. 1 a clock 80 comprising a pair of inverters 81 and 82. The output of inverter 81 is connected to the input of inverter of 81 by a pair of serially connected resistors 83 and 84, and is connected directly to the input of inverter 82. The output of inverter 82 is connected to the input of 82 through the serially combination of a capacitor 85 and resistor 83, and is directly connected to a count input terminal of clock counter 70.

There is also shown a one-shot multivibrator 90. Multivibrator 90 includes a two-input positive nor logic gate 91 having a first input 92 which is connected through a capacitor 93 to the output of inverter 69, and which is connected through a resistor 94 to a positive power input terminal 95. Output terminal 76 of counter 70 is connected to the input of an inverter 77 which has an output connected to another input 96 on gate 91. The output of 91 is connected through a diode 97 to the input of an inverter 101. The input of inverter 101 is connected to ground through a parallel combination of a capacitor 98 and a resistor 99. The output of inverter 101 is connected through a capacitor 111 to a reset input terminal on counter 70. The reset counter terminal of counter 70 is also connected to ground through a resistor 112.

There is also shown a pacer output pulse circuit 100. Circuit 100 includes an inverter 102 which has its input connected to the output of inverter 101 and its output connected through a resistor 103 to the base of a transistor 104. The collector of transistor 104 is connected through a resistor 105 to a power input terminal 106, and is connected through a capacitor 107 to an electrode terminal 108. The emitter of transistor 104 is connected to ground, and to an electrode terminal 109. Electrode terminals 108 and 109 are adapted to be connected to electrodes which are in turn adapted to be connected to the heart.

In FIG. 1 there is also shown output pulse width adjustment circuitry 120. Circuitry 120 includes a junction 121 connected through a serial combination of a diode 122 and a resistor 123 to terminal 46 of counter 40. Junction 121 is also connected through a serial combination of a diode 124 and a resistor 125 to counter output terminal 47, and through a serial combination of a diode 126 and resistor 127 to counter output terminal 48. Junction 121 is also connected to the input of inverter 101.

In FIG. 2 there are shown three graphs, *a*, *b* and *c* relative to the input signal to the pacer of FIG. 1. In graphs *a* and *b* it can be seen that the pulses for setting counter 40, pulses B, are preceded by a longer pulse A which is of a coded pulse width. Pulses A and B as received at receiver 10 comprise a burst of radio frequency pulses transmitted from a transmitter such as that shown in FIG. 3.

The burst of pulses comprising pulse A of graph *a* is received across coil 11 and capacitor 12, and the radio frequency components are filtered out by diode 13 and capacitor 14 such that pulse A of graph *b* is seen across resistor 15 to turn on transistor 16. The output of transistor 16 is felt at the input of inverter 21 and on input 38 of gate 36. Gate 36 has an output which is normally ZERO which will not change at this instant in time inasmuch as input 35 of positive nor gate 36 is held at a ONE due to the charge on capacitor 34. However, the input signal pulse A felt at the input to inverter 21 will cause its normally ZERO output to change to a ONE. The input of inverter 23 will not, however, ever, instantaneously change to a ONE, because of the charge time of capacitor 26 through resistor 22. Therefore, the output of inverter 23 will remain a ONE until a minimum time has passed for the charging of capacitor 26. This minimum time is set to be slightly less than the total time that input pulse A is present. Thus, pulses having a pulse width less than the minimum time set by resistor 22 and capacitor 26 will not affect the pacer operation.

After the minimum time has elapsed capacitor 26 will have charged sufficiently to cause the output of inverter 23 to go to ZERO. The switch of the output of inverter 23 from ONE to ZERO will cause capacitor 27 to commence charging through resistor 31. During the time of charge of capacitor 27, input 28 of gate 29 will temporarily be at the ZWEO level for a predetermined time. This predetermined period sets the maximum time for the coded signal A to affect the pacer. The output of inverter 21 is also felt on input 32 of gate 29 and as long as that output is a ONE, there will be no signal at the output of gate 29. However, if the output of inverter 21 changes back to a ZERO (input signal A ceases) during the predetermined time of the charge of capacitor 27, then the output of gate 29 will change to a ONE. Thus, if an extraneous noise signal occurs which is longer than the minimum time determined by capacitor 26 it may not be longer than the maximum time determined by capacitor 27 or it will still not affect the pacer. Input pulse A, as shown in graphs *a* and *b* is selected to end between the maximum and minimum times.

As stated above, when Pulse A ends the output of gate 29 will change from ZERO to ONE. This is felt through line 41 to reset counter 40, and will cause the discharge of capacitor 34 thus putting a temporary ZERO pulse on input 35 of gate 36. Input 35 will remain ZERO during the recharge time of capacitor 34 after input pulse A ends. This second predetermined period of time is selected to be just sufficient to open gate 36 for a period of time sufficient to put in the maximum number of count pulses to digital counter 40. As can be seen from graphs *a*, *b* and *c*, a plurality of count signals are transmitted, the number being determined by setting the transmitter, which are felt through receiver 10 on input 38 of gate 36 through line 39. As the input pulses change from ZERO to ONE state, the output of gate 36 will also change from state to state causing a counting of the pulses in counter 40. When the recharge of capacitor 34 has been accomplished, gate 36 will be shut off and the counting will end. The counted pulses will appear on count output terminals 42–45, which are connected, respectively, to one input on each of gates 51, 54, 57 and 61.

Clock 80 is continually sending a series of pulses to counter 70, and the count is appearing on terminals 72-75 which are also connected to gates 51, 54, 57 and 61. The output of gate 64 is normally a ZERO. However, when all four output terminals 42–45 of counter 40 match the respective output terminals 72–75 of counter 70 then each of the outputs of gates 51, 54, 57 and 61 will go to ZERO, thus causing all four inputs 65–68 of gate 64 to go to ZERO and causing the output of gate 64 to go to a ONE. This ONE is felt at the input of inverter 69 causing it to change to an output of ZERO, which output will be felt at the input to multivibrator 90.

As inverter 69 changes its output to ZERO, the changing pulse will be differentiated by capacitor 93 and resistor 94 to cause the leading edge to present a ZERO to input 92 of gate 91 thus enabling half of gate 91. However, the output of gate 91 will not change to a ONE unless input 96 is also at a ZERO. Input 96 will be held at a ONE by the output of inverter 77 as long as output terminal 76 of counter 70 is a ZERO. By se-

lecting terminal 76 to represent the next count after the highest represented by terminals 72–75 (for example, if terminal 75 represents the "8" count then terminal 76 is selected to represent "16" count of the digital counter 70) a minimum rate for the pacer output pulse can be established. It is therefore apparent that the first time that a pulse charge appears at the output of inverter 69, the leading edge of which is felt at input 92 of gate 91, there will be no change at the output at gate 91. However, the second time that terminals 72–75 of counter 70 match terminals 42–45 of counter 40 terminal 76 will have been switched to a ONE and input 96 at gate 91 will be disabled. Therefore, the second output of inverter 69 will cause at its leading edge, the output of gate 91 to change to a ONE. This change will be felt through diode 97 to commence the charge of capacitor 98 causing inverter 101 to have an output switch from the ONE to the ZERO state, representing the output of multivibrator 90. The time which the output of multivibrator 90 remains on and determined by the parallel combination of capacitor 98 and resistor 99, thus giving a predetermined output pulse width to the pacer output pulse. The output of multivibrator 90 is felt at inverter 102 to cause its output to go to a ONE. This causes the turn-on of transistor 104 and thus causes an output pulse to be applied to electrode terminals 108 and 109 which will be felt at the heart.

The output of multivibrator 90 is also felt through the combination of capacitor 111 and resistor 112 on the reset terminal of counter 70, such that the trailing edge of the output of inverter 101 causes a reset of counter 70. This reset will clear all of output terminals 72–76, thus disabling gate 91 and commencing the count cycle.

Thereafter, clock 80 will again cause counter 70 to receive pulses which will eventually again cause terminal 76 to be in the ONE state at the same time that output terminals 72–75 match the respective of output terminals 42–45 of counter 40. The number of pulses necessary to reach this state thus determined the rate at which pacer output pulses are provided to the heart. The count in set counter 40 will remain the same unless the operator uses the transmitter to set another count in counter 40, thus changing the rate. As has been pointed out above, only extraneous noise signals which coincidentally fall between the minimum and maximum times determined by the decoder 20 can enable the input to counter 40, and even should such a pulse occur the count will change only if this noise signal is followed by pulses which are completed during the time period determined by the charge time of capacitor 34. As most extraneous noise signals are of the 60 cycle per second variety, times have been selected which will prevent any reasonable possibility of such noise signals from changing the count in set counter 40 and thus affect the pacer rate. For example, pulse A has been selected to be 13 milliseconds to fall between a maximum and minimum gate time of 11 to 15 milliseconds as determined by capacitors 26 and 27 respectively. Thereafter, a maximum number of 127 pulses such as pulses B are completed within approximately 40 milliseconds, the pulses being approximately 100 microseconds wide with a repetition rate of approximately 250 microseconds.

Referring again to FIG. 1 a variation of the apparatus of this invention can be seen with regard to output pulse width adjustment apparatus 120. As has been explained above, the output pulse width is determined by the pulse time of multivibrator 90. The pulse time of one-shot multivibrator 90 is in turn determined by the parallel combination of capacitor 98 and resistor 99. Resistors 123, 125 and 127 have been provided so that the operator of the transmitter may select the output pulse width he desires by changing the count in counter 40. When any of output terminals 46, 47 or 48 are in the ZERO state then the respective of resistors 123, 125 and 127 will be in parallel with resistor 99. Thus, the operator may select an input count which, in addition to determining the rate by setting the states of terminals 42–45, will in addition set the states of terminals 46–48 to vary the resistance in multivibrator 90 to vary the output pulse width of the entire pacer. Diodes 122, 124 and 126 are provided to prevent a current flow into capacitor 98 when the respective of terminals 46, 47 and 48 are in the ONE state.

Referring now to FIG. 3, there is shown a transmitter which may be used to provide coded input information to the digitally controlled pacer of FIG. 1. In FIG. 3 there is shown a one-shot multivibrator 200. Multivibrator 200 includes a positive power input terminal 201 and a ground bus 202. A switch 203 has a first terminal 204 and a second terminal 205. Power terminal 201 is connected through a serial combination of a resistor 206 and a resistor 207 to terminal 204. Terminal 205 is connected to bus 202. A capacitor 208 is connected between terminals 204 and 205. Another capacitor 209 is connected from terminal 204 to the input of an inverter 211. The input of inverter 211 is also connected to a junction between resistors 206 and 207. The output of resistor 211 is connected through a diode 212 to another inverter 213. A parallel combination of a capacitor 214 and a resistor 215 is connected between the input of inverter 213 and bus 202.

In FIG. 3 there is also shown oscillator control circuitry 220. Circuitry 220 includes an inverter 221 which has an input connected to the output of inverter 213 and an output connected to an input 222 of a two-input positive NOR logic gate 223. The output of gate 223 is connected to the input of another inverter 224. Yet another inverter 225 has an output connected to an input 226 of gate 223. Inverter 225 has its input connected to a positive power input terminal 227 through a resistor 228. The input of inverter 225 is also connected to one side of a capacitor 229.

There is also shown an oscillator 230 which has an input connected to the output of inverter 224 and an output connected to a transmitting coil 231. Coil 231 is adapted to transmit signals that will be received by coil 11 of receiver filter 10 described in the discussion of FIG. 1 above.

FIG. 3 also discloses a locking gate 240 which includes a two-input positive NOR logic gate 241. Gate 241 has an input 242 connected through a capacitor 243 to the output of inverter 213, and connected to a resistor 244 to bus 202. Another two-input positive NOR logic gate 246 has an input 247 connected to the output of gate 241. The output of gate 246 is connected to an input 245 on gate 241.

There is also shown a gated clock 250. Cock 250 has a two-input positive NOR logic gate 251 which has an output connected to the input of an inverter 252. The output of inverter 252 is connected to the other plate of capacitor 229 and by a serial combination of a capacitor 253 and a resistor 254 to an input 255 of gate

251. A resistor 256 is connected from a junction between capacitor 253 and resistor 254 to the input of inverter 252. Another input 257 of gate 251 is connected to a positive power input terminal 258 through a capacitor 259. Input 257 is also connected through a resistor 261 to the output of gate 241. A diode 262 is connected across resistor 261.

FIG. 3 also shows an output pulse counter 270. Counter 270 has a reset input terminal connected to the output of inverter 221, and a count input terminal connected to the output of invertor 225. Counter 270 also has a plurality of output terminals 271, 272, 273, 274, 275, 276 and 277.

Also shown in FIG. 3 is a pacer rate control circuitry 280. Circuitry 280 includes a multi-positional switch 281 and a plurality of diodes such as 282 connected in a predetermined sequence to output terminals 274, 275, 276, 277 on counter 270.

Also shown is a pacer output pulse control circuitry 290 which includes a multi-positional switch 291 and a plurality of diodes such as 292 connected in a predetermined configuration to output terminals 271, 272, 273 on counter 270.

The wiper arms of switches 281 and 291 are connected to a bus 301. Bus 301 has a first end connected through a resistor 302 to a positive power input terminal 303. A second end of bus 301 is connected to the anode of the diode 304. The cathode of diode 304 is connected to ground through a resistor 305 and to an input 248 on gate 246.

The operation of the transmitter of FIG. 3 is commenced by the closure of switch 203 which may be accomplished either manually or automatically. This causes the input of inverter 211 ot go to a ZERO. The input of inverter 211 had been at a ONE due to the effect of the RC network comorising resistors 206 and 207 and capacitors 208 and 209, being connected between bus 202 and positive input terminal 201. This change from ONE to ZERO of the input of inverter 211 will cause its output to change from a ZERO to a ONE. This will be felt through diode 212 across the parallel RC network comprising capacitor 214 and resistor 215, and on the input of inverter 213. The output of inverter 213 will therefore change from a ONE to a ZERO and remain a ZERO for a time determined by the RC time constant of capacitor 214 and resistor 215. This time is chosen to be the pulse width A shown in FIG. 2*a* and *b*, which in the specific configuration mentioned above would be 13 milliseconds to fall between the gated on time of 11 to 15 milliseconds provided in decoder 20 described in the above discussion of FIG. 1.

When the output of inverter 213 goes to ZERO this change will be felt on the input of inverter 221 of oscillator control circuitry 220. This will cause an output change from ZERO to ONE at inverter 221 thus causing a positive signal to appear at input 222 of gate 223. The output ONE at inverter 221 is also felt at the reset terminal of counter 270 to reset all of its output terminals to ZERO. The positive input will cause positive NOR logic gate 223 to have an output change from ONE to ZERO. This change will be felt at the input of inverter 224 causing its output to go from ZERO to ONE. The positive going signal at the output of inverter 224 will turn on oscillator 230 thus causing a burst of pulses to appear on coil 231. The oscillator 230 will remain on until the output signal of one-shot multivibrator 200 returns to its original state, in the manner described above. Thus, the output of inverter 213 will return to ONE, the output of inverter 221 will return to ZERO, which change will be felt on the input of gate 223 causing it to return to ONE state, thus causing the output of inverter 224 to return to the ZERO state to shut off oscillator 230. It will thus be apparent that the burst of pulses on coil 231 will be present for a period of time determined by multivibrator 200, to produce the coded burst of pulses shown at A in FIG. 2 *a*.

The trailing edge of the output pulse from multivibrator 200, that is the return of the output of inverter 213 to the ONE state, will be felt across a differentiator comprising capacitor 243 and resistor 244 thus causing a positive signal to appear at input 242 of gate 240. This positive input will cause positive NOR logic gate 241 to change its output from a ONE to a ZERO. This change is felt at input 247 of gate 246 causing its output to change from a ZERO to a ONE. This positive output of gate 246 is connected to input 245 of gate 241 and locks on gate 241 so that its output remains a ZERO. The effect of input 248, which is normally a ZERO, on locking gate 241, will be described below.

When the output of gate 241 changes to ZERO, this will be felt through resistor 261 to gate on clock 250 by changing the input 257 of gate 251. The gated clock 250 then operates at a predetermined frequency, providing a square wave output in a manner well known to those of reasonable skill in the art.

The output of clock 250 is felt through the RC network of capacitor 229 and resistor 228 on the input to inverter 225. The negative going edges of the square wave output will cause the output of inverter 225 to change from its normal ZERO to a ONE. However, the period of time that this change remains is determined by the RC time constant of capacitor 229 and resistor 228, and thus the pulse width as shown in B of FIG. 2 *a* and *b* is determined. In the specific example given above, this pulse width is chosen to be 100 microseconds. This change in output of inverter 225 from a ZERO to a ONE is felt at input 226 of gate 223, and at the count input terminal of counter 270 where it is counted. The result of the positive input at 226 of gate 223 is a change from ONE to ZERO at the output of gate 223 thus causing a change from ZERO to ONE at the output of inverter 224. The positive signal out of inverter 224 will turn on oscillator 230 to provide a burst of pulses at coil 231. This burst of pulses will be on for a period of time determined as described above by capacitor 229 and resistor 228. Thus, short bursts of pulses are transmitted by coil 231 as shown at B in FIG. 2*a*. The pulse repetition rate is determined by clock 250.

As has been described in the discussion of FIG. 1, set counter 40 receives a predetermined number of pulses as shown in FIGS. 2*a* – *c*, and having counted these pulses, then provides outputs at terminals 42 – 48, from which the pacer rate and pulse width are determined. The transmitter of FIG. 3 allows the programming of the pulses into set counter 40 of FIG. 1 through the use of switches 281 and 291, which in conjunction with diodes 282 and 292 and counter 70 determine, respectively, pacer pulse rate and pacer output pulse width. As noted above, counter 270 is reset to an all ZERO state at the time the transmitter sends the code pulse A. Whereafter, when pulses B are being sent, the pulsing output of inverter 225 is received and counted by 270. The wiper arm of, for example, switch 281 will be con-

nected through selected one or more of diodes 282 to the selected ones of counter output terminals 274–277. Following the reset of counter 270, all of outputs 274–277 would be in the ZERO state. Thus, current flow will be felt from power input terminal 303 through resistor 302, through the selective of diodes 282, to the ZERO state at the respective of terminals 274 – 277. Thus, the anode of diode 304 will be in the ZERO state and a ZERO will be felt at input 248 of gate 246, thus keeping the output of gate 246 at a ONE and locking in the ZERO output of gate 241 as described above.

The operation of switch 291, to determine pacer output pulse width operates in the same manner, such that selective of diodes 292 will connect bus 301 to a ZERO until such time as the selective of counter outputs 271 – 273 have all reached a ONE state.

When the output pulses from the transmitter have reached a perdetermined count as determined by counter 270 so that, in the switch selection shown in FIG. 3, for example, all of counter terminals 274 – 277 are in the ONE state, then the positive signal will be felt on the anode of diode 304 causing a ONE signal to appear on input 248 of gate 246. This in turn will cause the output of 246 to go to ZERO, which in turn will be felt at input 245 of gate 241. As input 242 of gate 241 is also in the ZERO state, the output of gate 241 will return to the ONE state. This in turn will be felt on input 247 of gate 246 to lock its output into the ZERO state, thus locking gate 241 into an output ONE state. The output ONE from locking gate 240 will be felt across the combination of capacitor 259, resistor 261 and diode 262 to turn off gate 251 thus shutting down gated clock 250.

In summary, the count of pulses B may be selected through the use of switches 281 and 291. When that count has been reached, the transmitter is turned off and no further pulses are sent. The pulses B will have been received by the pacer shown in FIG. 1, and have properly passed through receiver-filter 10 and decoder 20 to be stored in set counter 40. Set counter 40 is then compared with counter 70 to determine pacer pulse rate and output pulse width.

Referring now to FIG. 4, there is shown a variation of a portion of the pacer apparatus of FIG. 1. FIG. 4 includes a set counter 440 having a reset terminal connected to a terminal 439 adapted to receive the coded reset signal as described in the pacer apparatus of FIG. 1. Counter 440 also has a count terminal connected to a terminal 438 adapted to receive the coded input data, as described in the pacer apparatus of FIG. 1. Counter 440 includes a plurality of output terminals 441, 442, 443, 444, 446, 447 and 448.

FIG. 4 also shows a clock counter 470 having a count terminal connected to a clock 480. Counter 470 also has a reset terminal connected to the output of an inverter 437 which has an input connected to the output of three-input positive NOR logic gate 436. Gate 436 has three inputs, 433, 434, and 435. Input 433 is connected to a terminal 431 adapted to receive an external reset signal, for example, to make the pacer apparatus a demand pacer apparatus. Input terminal 434 is connected to a terminal 432 adapted to be connected to a coded reset input, the same as input terminal 439 described above. Input 435 of gate 436 is connected to the output of an inverter 481. Counter 470 includes output terminals 471, 472, 473, 474, 475, 476, 477, 478 and 479.

There is also shown a pulse rate comparison circuit 450 and a pulse width comparison logic circuit 490, each of which is connected to both of set counter 440 and clock counter 470 for comparing the outputs of the two counters.

Logic circuit 450 includes four two-input exclusive OR gates 451, 454, 457 and 461, as well as a four-input positive NOR logic gate 464, an inverter 469, and a two-input positive NOR logic gate 481.

Gate 451 has an input 452 connected to output 441 of counter 440, and an input 453 connected to output 478 of counter 470. Gate 454 has an input 455 connected to output 442 of counter 440, and an input 456 connected to output 477 of counter 470. Gate 457 has an input 458 connected to output 443 of counter 440, and an input 459 connected to output 476 of counter 470. Gate 461 has an input 462 connected to output 444 of counter 440 and an input 463 connected to output 475 of counter 470. Gate 464 has an input 465 connected to the output of gate 451, an input 466 connected to the output of gate 454, an input 467 connected to the output of gate 457 and an input 468 connected to the output of gate 461. The output of gate 464 is connected to the input of inverter 469. Gate 481 has an input 482 connected to the output of inverter 469 and an input 483 connected to the output of inverter 429.

Referring again to the pulse width comparison logic 490, it is seen that gage 491 has an input 492 connected to the output 445 of counter 440, and an input 493 connected to output 474 of counter 470. Gate 494 has an input 495 connected to output 446 of counter 440, and an input 496 connected to output 473 of counter 470. Gate 497 has an input 498 connected to output 447 of counter 440, and an input 499 connected to output 472 of counter 470. Gate 501 has an input 502 connected to output 448 of counter 440, and an input 503 connected to terminal 471 of counter 470.

Gate 504 has an input 505 connected to the output of gate 491, an input 506 connected to the output of gate 494, an input 507 connected to the output of gate 497 and an input 508 connected to the output of gate 501.

There is also shown in FIG. 4 a locking gate 510, including a pair of two-input positive NOR logic gates 511 and 515. Gate 511 has an input 512 connected to a terminal 518 adapted to be connected to output pulse circuitry for providing a pulse to electrodes adapted to be connected to the heart. Gate 511 also has an input 513 connected to the output of gate 481 and to input 435 of gate 436. Gate 515 has an input 516 connected to the output of gate 511 and to a terminal 519 also adapted to be connected to output pulse circuitry. Gate 515 also has an input 517 connected to the output of gate 504. The output of gate 515 is connected to input 512 of gate 511.

To understand the operation of the embodiment of FIG. 4, it should be recognized that means such as receiver-filter 10 and decoder 20 are used to provide a coded reset to each of counters 470 and 440, and to provide the coded data to memory or set counter 440. Therefore, counter 440 contains selected information relative to pacer rate and pulse width, as was true in the embodiment of FIG. 1. Clock counter 470 receives continuous pulses from clock 480, and when the count in counter 470 compares with that stor[illegible]et counter 440, this will be recognized by the separ[illegible]omparison

logic circuits 450 and 490. Counter 470 has its output 479 connected to the inverter 429 for the purposes of establishing a minimum rate for the pacer as did output terminal 76 of counter 70 in FIG. 1.

Referring to the operation of the rate selection circuitry, the outputs of exclusive OR gates 451 – 461 will each be in the ONE state whenever their inputs are not the same. Thus, when the reset of counters 440 and 470 occurs, all of the inputs to gates 451 – 461 will be the same and an output change from each gate will occur. However, output terminal 479 of counter 470 will be reset to ZERO causing a ONE to appear at input 483 of Gate 481 thus inhibiting an output at that time.

As soon as counter 440 starts to count the coded data which immediately follows the coded reset, all of the inputs to each of gates 451 – 461 will not be the same and at least one of such gates will have an output ONE. This one will be felt on the input of gate 464 to keep its output at a ZERO, which causes a ONE to be felt on input 482 of gate 481 causing its output to be a ZERO.

As clock 480 continues to be counted by counter 470, the output of counter 470 on terminals 475 and 478 will eventually compare with those on terminals 441 – 444 of counter 440. However, output 479 will still be a ZERO thus keeping the output of gate 481 at a ZERO and this first comparison of counters 440 and 470 will not result in a signal to the output pulse terminals 518 and 519. Assuming output terminal 479 is the highest count number to be used in the system shown, when clock 480 has been counted to a predetermined value, terminal 479 will switch to a ONE, thus enabling the output gate 481 of comparison circuitry 450. Counter 470 will continue to count clock pulses until terminals 475 through 478 compare with terminals 441 through 444 of counter 440. Thus, the coded input data to counter 440 determines the pacer rate, with terminal 479 of counter 470 determining a minimum rate.

With gate 481 enabled, and with a comparison between terminal 475 – 478 and 441 – 444, all outputs of gates 451 – 461 will go to ZERO thus causing the output of gate 464 to go to a ONE. This one will be felt through inverter 469 to be a ZERO on input 482 of gate 481. As input 483 is also held at a ZERO due to inverter 429 and output terminal 479, the output of gate 481 will switch from its normal ZERO to a ONE state. This ONE will be felt on input 513 of gate 511 and on input 435 of gate 436 to reset counter 470.

The positive signal on input 513 will cause the output of gate 511 to switch from a ONE to a ZERO. This will cause the output of gate 515 to switch from a ZERO to a ONE, which effect will be felt both on output terminal 518 and on input terminal 512 at gate 511 to lock gate 511 to an output ZERO state. Thus, terminals 518 and 519 are switched into the outputs states and locked into those states by locking gate 510.

As stated above, at the time the output signal commenced a reset signal was felt on input 435 of gate 436 to reset counter 470. This has the effect of again disabling comparison logic circuitry 450 by resetting output 479 to ZERO and of starting the count process over again for counter 470. When sufficient clock pulses have been counted by counter 470 for outputs 471–474 to compare with outputs 445 – 448 of counter 440, then the outputs of each of gates 491 – 501 of comparison logic circuitry 490 will switch to the ZERO state. This causes gate 504 to have an output switch from its normal ZERO to a ONE state. This ONE is felt on input 517 of gate 515 to unlock its output from the ONE state to the ZERO state. This ZERO is felt on output terminal 518 and on the input 512 of gate 511 to lock circuitry 510 into its original state and turn off the output pulse. Thus, the output pulse width is obtained by comparison of portions of counters 440 and 470, in the same way that pulse rate is determined.

It will be apparent that the above described action is repeatable for permanent automatic stimulation of the heart. The minimum pulse rate will be determined by output terminal 479 and its count level, while the adjustable pacer output pulse rate will be determined by an input to memory 440. Each time memory 440 commences a pulse, that pulse will be stopped after a period of time determined by another portion of memory 440 being compared with the count and clock counter 470.

It should also be recognized that means for sensing cardiac beats can be used to provide a reset signal to external reset terminal 431. These means are well known to those skilled in the art, and would result in the pacer in FIG. 4 being switched to use as a demand pacer, because a timed reset from normal cardiac operation to counter 470 would keep terminal 479 in the ZERO state thus preventing the commencing of any output pulse for artificial stimulation of the heart.

It has also been recognized that a much finer selection of pulse rate and pulse width can be achieved by using counters having, for example, 14 states in combination with a clock such as clock 480 having an output frequency in excess of 15,000 Hz.

From the foregoing descriptions of the preferred embodiments of this invention, it will be apparent that the apparatus is indeed useful for medical-electronic devices other than cardiac pacers. It is not intended that the scope of this invention be so limited. It will also be apparent that that portion of the apparatus, for example, which is used to selectively store information for determining and changing pulse width can be used for varying other perameters of the pacer output pulse. For example, counter 40 output terminals 46 – 48 could be connected to a series of batteries which supply power for the output pulse, and could selectively switch certain of the batteries in series with each other according to the information stored in counter 40, to thus vary the amplitude of the output signal.

What is claimed is:

1. Electro-medical stimulation apparatus comprising: first and second binary data storage means; means for selectively changing data stored in the first storage means; means for continually changing data stored in the second storage means at a predetermined rate; means for comparing at least portions of data stored in the first and second storage means and for providing signals in the presence of a predetermined comparisons; and means connected to receive the signals from the means for comparing for providing stimulation signals.

2. The apparatus of claim 1 including: means connected to the first storage means for controlling the width of the stimulation signals according to at least a portion of the data stored in the first storage means.

3. The apparatus of claim 1 including: means connected to the first storage means for controlling the amplitude of the stimulation signals according to at least

a portion of the data stored in the first storage means.

4. The apparatus of claim 1 in which the means for selectively changing the data stored in the first storage means includes: receiver and decoder means connected to the first storage means.

5. The apparatus of claim 4 including the combination: transmitter and encoder means for transmitting coded signals to the receiver and decoder means.

6. The apparatus of claim 1 including: further means for comparing at least other portions of data stored in the first and second storage means and for providing a signal in the presence of a predetermined comparison; means connecting the further means for comparing to the means for providing a stimulation signal; and the means for providing a stimulation signal having means responsive to a signal from the means for comparing for starting a stimulation signal, and having means responsive to a signal from the further means for comparing for stopping the stimulation signal.

7. Apparatus for providing electro-medical stimulation pulses comprising: clock means having a pulsed output signal; first counter means connected to count the output of the clock means; further counter means for receiving and storing a predetermined count; comparison logic means for continually comparing the counts in the first and further counter means to provide a polarity of signals; and stimulation circuit means controlled by the plurality signals for providing stimulation signals.

8. The apparatus of claim 7 including: means for receiving pulse signals; and means connecting the means for receiving to the further counter means.

9. The apparatus of claim 8 including: means for transmitting pulse signals; and means connected to the means for transmitting for varying the number of pulses transmitted.

10. The apparatus of claim 9 including: means connected to the means for transmitting for encoding the transmitted pulse signals; and means connected to the means for receiving for decoding the transmitted pulse signals.

11. Digital apparatus for electro-medical stimulation comprising: first binary counter means having input terminal means, reset terminal means and output terminal means; second binary counter means having input terminal means and output terminal means; data input means connected to the first counter input terminal means and reset terminal means; binary clock means connected to the second counter input terminal means; logic circuit means having input terminal means and output terminal means; means connecting a portion of the first and second binary counter output terminal means to the logic circuit means input terminal means; output circuit means adapted to be connected to a portion of a body; and means connecting the logic circuit means output terminal means to the output circuit means.

12. The apparatus of claim 11 in which said second binary counter includes reset terminal means connected to said output circuit means.

13. The apparatus of claim 11 including: inhibit means included in the output circuit means further of the second binary counter output terminal means connected to the output circuit means inhibit means for inhibiting operation of the output circuit means until a minimum count is reached in the second binary counter means.

14. The apparatus of claim 11 including: output pulse width control means; and means connecting the output pulse width control means between the output circuit means and a further portion of the first binary counter output terminal means.

15. The apparatus of claim 14 in which the output pulse width control means comprises: monostable multivibrator means, means for adjusting the period of oscillation of the monostable multivibrator means; and means connecting the means for adjusting to the further portion of the first binary counter output terminal means for controlling the period of oscillation according to the binary states of the further portion of the first binary counter output terminal means.

16. The apparatus of claim 11 in which the logic circuit means includes: a plurality of logic gates having input terminal means and output terminal means; each of the logic gates having a portion of its input terminal means connected to a portion of the first binary counter output terminal means, and having a further portion of its input terminal means connected to a portion of the second binary counter output terminal means; and means connecting the logic gates output terminal means to the logic circuit means output terminal means.

17. The apparatus of claim 11 including: second logic circuit means having input terminal means and output terminal means; means connecting a further portion of the first and second binary counter output terminal means to the second logic circuit means input terminal means; and means connecting the second logic circuit means output terminal means to the output circuit means.

18. The apparatus of claim 17 in which the output circuit means includes: means responsive to the logic circuit means for starting an output signal; and means responsive to the second logic circuit means for stopping the output signal.

19. The apparatus of claim 11 in which the data input means includes: RF receiver and decoder means.

20. The apparatus of claim 19 including in combination: RF transmitter and encoder means.

21. The apparatus of claim 20 in which the RF transmitter and encoder means includes: enabling means; RF oscillator means having a transmission coil; code logic means connecting the enabling means to the oscillator means for providing a first timed period of oscillation when the enabling means is actuated; further binary counter means; further binary clock means; means connecting the further clock means between the enabling means and the further counter means and to the code logic means; means connecting the further counter means to the code logic means; means for commencing a plurality of further timed periods of oscillation in response to the output pulses of the further clock means; means connected to the further counter means for stopping the further timed periods of oscillation until the enabling means is again actuated; and selection means connected to the further counter means for selecting a desired number of the further timed periods of oscillation.

22. The apparatus of claim 21 in which the RF receiver and decoder means includes: means for detecting the first timed period of oscillation; further code logic means connected to the means for detecting and

enabled thereby only where a pulse of the first timed period and frequency of oscillation is detected; the means for detecting and the further code logic means also for detecting the further timed periods of oscillation and for providing a binary count signal to the input terminal means of the first binary counter means for each such further timed period occurring within a predetermined time.

23. In implantable cardiac pacer apparatus, including electrode means adapted to be connected to a heart and circuit means for providing electrical impulses on the electrode means, the improvement comprising: electrical storage means for storing programs and having at least first and second storage portions; means for receiving remotely sent programs connected to the first storage portion; clock means; means connecting the clock means to the second storage portion; means for comparing programs stored in the first and second storage portions for providing signals; means for connecting the means for comparing between the first and second storage portions and the circuit means, for controlling the electrical impulses according to the stored program; and all said means encapulated in means substantially inert to body fluids and tissue.

24. The apparatus of claim 23 in which the means for receiving remotely sent programs comprises: means for receiving and decoding transmitted RF signals.

25. The apparatus of claim 24 including in combination: means for transmitting coded RF signals representative of a storable electrical program.

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